PhD-FSTC-2017-69
The Faculty of Sciences, Technology and Communication

DISSERTATION

Defense held on 24/11/2017 in Luxembourg

to obtain the degree of

DOCTEUR DE L'UNIVERSITÉ DU LUXEMBOURG

EN SCIENCES DE L'INGÉNIEUR

by

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ACTIVE HARMONICS COMPENSATION IN SMART GRIDS

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Abstract

About fifty years after the beginning of the oil era, end of the industrial revolution period, the development of the electricity production techniques, transmission and distribution systems will have a big footprint in the technological and scientific progress. From that time, the electrical energy will steadily be more and more important to the economic and social improvement and has become even a very strong development progress indicator for all the countries. The trend shows that all the countries are consuming more and more energy in form of electricity. Day after day, the electric power system is expanding and evolving. Although the quantitative requirements can easily be achieved, the qualitative requirements are, in contrast facing serious challenges.

Every electrical device is built to work under specific conditions like the voltage and current levels, and the surrounding temperature. Once these rated conditions are reached, the device is operating properly as indicated by the constructor. Any deviations from these rated conditions can, and surely will, make the appliance functional behaviour appear different from what is expected. In order to ensure that electrical appliances work properly (this can be defined in terms of output voltage and current, temperature, lifetime etc…), the electricity market made of the electricity consumers (who are the owners of the electrical appliances) and the electricity producers-distributors entity need a common agreement on the supply voltage that meets these special criteria. The Power Quality (PQ) refers to how closely the characteristics of the supplied voltage meet that of the rated, standard market-defined, electrical power voltage. However, the power system receives energy generated from multiple historically conventional (thermal, hydraulic) and recent non-conventional (wind, solar, tides) sources. It also has to satisfy the demand of the continuous growing use of sophisticated modern power electronic devices that require a good PQ. Therefore, over the decades, the quality of the electrical energy has become a crucial issue for the energy producers and distributors as well as for the end users. Customer surveys worldwide have shown that the number of complaints on disturbances related to the PQ is increasing year after year. Poor PQ may lead to a variety of technical problems that goes from little dysfunction, overheating or fast ageing of devices and installation, up to large material damages that generally cause very large financial losses. This is not only on the customer side but also for the network operator, who is affected by issues such as the transmission cables and transformers.

The breakthrough of electronics, which improved the whole goods and material production chain (from mineral extraction to the final product), is undeniable. It results in the production and worldwide use of more and more electronic-powered devices, a considerably great help in the management, control, security, maintenance and monitoring of the power production and distribution system. However, when these sophisticated electronic components are used as electrical consumers (built in our daily used electric appliances), they distort the supply voltage and thus they unfortunately degrade the PQ. One real paradox is that these electronic-based electrical devices are very sensitive to the poor PQ. This degradation of the PQ caused by the electronic components is due to their intrinsic non-linear behavior, characterized by a non-sinusoidal drawn current waveform despite the pure sinusoidal supply voltage feeding them. Among many other problems degrading the PQ in a power grid, these non-linear loads

generate current and voltage harmonics. These generated harmonics, if not eliminated, can be so high that they exceed the limits imposed by the rules guiding the electricity market.

Keeping in mind one of the world's challenges of the millennium is to reduce the ecological impact of the human activities, minimising the level of the harmonics pollution, while maximally exploiting the available decentralized energy produced from renewable sources, represents a good contribution to the international objectives. The combination of different types of locally used renewable energy sources with a guaranteed PQ leads to fewer energy losses over the long utility grid lines. This inevitably reduces the global financial cost of energy (less equipment's damages and longer lifetime due to better working conditions). All these issues define the technological and economic context, which leads to the research project presented here.

Summary

This work presents firstly the different problems, which may affect the performance of the power supply in terms of reliability and quality: What are the global measures and indices used to quantify the power quality? What are the major guidelines recommended by the different national standards worldwide? Secondly, the work focuses on the different PQ degradation factors with an emphasis on harmonics. A general overview of the multiple causes of harmonics is then given, in particular regarding their consequences concerning not only the energetic aspect but also the economic one and the equipment. Afterwards, different existing passive, as well as active mitigation technics against these harmonics pollution, are described with a particular attention given to the precise detection methods. These methods include the major frequency domain methodology, which is the Fast Fourier Transform, and the PLL, which is the most popular time-domain methodology. Different improvement techniques for the existing single-phase "delay-dq PLL" are then presented followed by the proposal of a new single-phase PLL, whose basic structure relies on the synchronous reference frame transformation (dq-transformation).

The main objective of the work focuses on the development of a voltage active power filter implementing a new selective harmonics compensation algorithm. The first design is described as follows: Finite impulse response band-pass filters decomposing the measured voltage signal as a sum of different harmonics voltages, including the fundamental component; PLLs (frequency-tuned) transform of the oscillating signals into two orthogonal and rotating components (dq-transform). The dq-components of each harmonic are controlled to zero into its PLL frame using standard PI-controllers and the compensating harmonics waves are generated via the inverse PLL. All the harmonics compensating waves are superimposed and added to the fundamental reference signal. This end result represents the final control signal of the inverter. Implemented in the MATLAB-SIMULINK simulation environment, this foreseen methodology depicted as major issue the control stability especially when the system frequency differs from the rated one. This is the reason why a second design has been proposed. The main improvement is done on the harmonics detection stability by replacing the PLLs frames by the well-known internal frame of the fundamental voltage of the controlled inverter. After the convincing theoretical results from the simulations, the method is implemented and validated experimentally on a test rig in the lab.

The two key features of the developed active power filter (APF) are:

- Its potential use as a standalone power unit that compensates by itself the harmonics that could appear in the system while generating the fundamental voltage necessary to build up the micro-grid.
- Its potential to serve as a full grid-tied power element that not only mitigates the voltages harmonics on the coupled grid but also supports the grid by controlling the exchanged active and reactive powers between the inverter and the grid.

Dedicated to my beloved parents Daniel and Lucie NGANI.

For your love, encouragement and inspiring beings…

Acknowledgments

This project is realized in the Research Unit in Engineering Sciences (RUES) at the University of Luxembourg. It is supported by the Luxembourg National Research Fund (FNR) under the AFR Grant 8043977. I would like to express my deep gratitude to the FNR for believing in me by funding this project. I am very grateful for the great opportunity offered.

The University of Luxembourg is the institution that has built my complete higher academic curriculum. From 2007 to 2017, I have completed my Bachelor, then my Master and finally my PhD degree. I am very thankful to the University of Luxembourg for hosting me and providing me all the necessary guidance to realize my potential.

I am very grateful to my supervisors and members of my Dissertation Supervisory Committee for their support. To my main supervisor, Professor Jean-Régis Hadji-Minaglou, I am very grateful for being the initiator and the guide of this research project. Your advices had a significant impact on the progress and the final quality of this work. Thank you for your support, patience, understanding and accessibility.

I would like to express my gratitude to my sisters and brother for the peaceful atmosphere, happiness and all the encouraging messages I have been surrounded with.

Thank you to Maman Elisabeth Keou for being a great mentor for my parents. I consider myself very lucky to have had the chance to know you since my childhood. Your peace of mind is inspiring me every day.

To my beloved Ariane, you are the one with whom I have shared most of the time during this project. Thank you for being a listening ear for me. You have provided me an invaluable stability which has helped being at my best for this research project. I am very grateful for that.

To my basketball club BBC MAMBRA and in particular, my Coach and teammates, being with you all these years is one of the best enrichment experience I ever had. From the assiduity to weekly practices to the organization of non-sportive events, I have learned a lot with you.

Finally, I would like to thank all my friends and relative for your encouragements.

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Table of Contents

Table of figures

List of tables

Acronyms

AC	Alternating current
APF	Active power filter
CSI	Current source inverter
DC	Direct current
DQ	Direct-quadrature
DSP	Digital signal processor
EHV	Extra high voltage
FFT	Fast Fourier transform
FIR	Finite impulse response
FPGA	Field-programmable gate array
GTO	Gate turn-off thyristor
HPF	High-pass filter
HV	High voltage
IGBT	Insulated-gate bipolar transistor
IIR	infinite impulse response
LC	inductive-capacitive
LPF	Low-pass filter
LV	Low voltage
MOSFET	Metal-oxide-semiconductor field-effect transistor
MV	Medium voltage
P	Active power
PI	Proportional-integral
PCC	Point of common coupling
PLL	Phase-locked loop
PQ	Power quality
PWM	Pulse-width modulation
Q	Reactive power
RLC	Resistive inductive and capacitive
RMS	Root-mean-square
S	Apparent power
STATCOM	Static synchronous compensator
SVM	Space vector modulation
THD	Total harmonic distortion
TDD	Total demand distortion
UPQC	Unified power quality conditioner
VSI	Voltage source inverter
VI	Virtual instrument

1 Electrical Power Supply: Reliability and Quality

Electricity is certainly one of the most important raw input material for the industry. Compared to other types of energetic raw materials like natural gas, coal, petroleum and even non-energetic inputs like cotton, timber, corn etc…, electricity is an uncommon product because it is a steady flow of material (electrons), invisible, intangible and hardly storable in large quantity. The only possibility is to quantify its presence using electrical measurement sensors like voltmeters and ampere meters of which principles are based on the physical manifestation of the electricity. A long time ago, the most important concern of the electricity consumers was whether electric power was present or not, and how long it will last without any interruption. This is the continuous availability character of a good electric supply, i.e. the reliability.

1.1 Supply reliability

Still the most important nowadays, the reliability of power supply has been considerably improved, but not completely resolved. Nevertheless, the impediments to a 100% reliable power supply today are quite different from those in the past. The devices and equipment failure, essentially due to the poor quality of the materials and the components, was the main cause of the low supply reliability. In addition to this, occur natural phenomena like lightning and short-circuits caused by animals (rats, birds) or fallen trees. Nowadays, the protection materials and technics against lightning are more efficient and the routing equipment (used to continue supplying a part of the power grid by passing through surrounding lines when the dedicated supplying line for that sector is down) are also better, although problems like blown fuses, breakers opening, or control malfunction, are still existing. It will be very hard to completely get rid of them, simply because there is always some manufacturing non-accuracy that can lead to slight function deviations.

1.1.1 Types of reliability problems

Based on the reliability concept described above, the main and only one problem of reliability are interruptions: a complete absence of the supply voltage. For every country standard, the definition of the supply interruption may vary slightly, and the common differentiation variable is the duration of the interruptions.

The European standard EN-50160 [1] [2] distinguish two types of interruptions:

- Short interruptions: defined as a supply voltage lower than 1% of the nominal voltage and this from 10ms up to 3 minutes.
- Long interruptions: The only difference with the short ones is that the interruption time exceeds 3 minutes.

For the IEEE-1250 standard in the US [1] [2], once the voltage amplitude is less than 10% of the nominal value, there are

- Instantaneous interruptions: last between 0.5 and 30 cycles (8.3 to 500 milliseconds).
- Momentary interruptions: last from 30 cycles to 2 seconds.
- Temporary interruptions: last from 2 seconds to 2 minutes.
- Sustained interruptions: last longer than 2 minutes.

The Australian standard [3] is apparently stricter concerning the durations than the US and Europeans ones. It distinguishes:

- Momentary interruptions: the interruption time goes from half cycle to 3 seconds.
- Temporary Interruptions: the shortage time varies between 3 seconds and one minute.
- Sustained interruptions: the interruption lasts more than one minute.

The South-African standard [4] uses an additional differentiation criterion: the voltage level of the power supply.

- Momentary interruptions: when, for EHV and HV, the voltage shortage last from 3 to 60 seconds but for MV and LV the duration varies between 3 seconds to 5 minutes.
- Sustained interruptions: the shortage duration for EHV and HV network lasts more than 60 and more than 5 min for MV and LV systems.

1.1.2 Power reliability indicators

According to the IEEE Standard 1366 [5], it exists a sufficient number of reliability indices that are used to track the reliability performance. They are typically defined as a function of the frequency of interruptions, the duration of the interruption measured in seconds, minutes, hours or even days, the number of customers. The most common ones are SAIDI, CAIDI and CAIFI [6] [7] [8].

- SAIDI: System Average Interruption Duration Index. This index gives the information concerning the average time during which the customers had no supply voltage. More commonly known as the average customer minutes off supply, it is generally calculated over a period of one year as the sum of all the interruptions duration multiplied by the number of the interrupted customers for each interruption, divided by the total number of customers. Here, the total number of interruptions considered includes not only the unplanned interruptions but also the planned ones. A SAIDI of 15 minutes means that customers connected to a power feeder experienced in average 15 minutes of no supply in a 12 months period.
  Let us consider the following example. On the 15th day of the month, four outages were recorded on a utility grid serving 20000 customers. The Table 1-1 below shows how the SAIDI is calculated for that day.

Table 1-1: SAIDI Calculation at a Specific Day with Outages

Date	Time	Interrupted Customers	Duration in minutes	Customers-hours
15th	08:20	100	90	150.00
15th	14:05	25	20	8.33
15th	14:50	400	45	300.00
15th	19:37	30	80	40.00
Total [customer-hours]				498.33
SAIDI [min]				1.495

For each interruption event, the customers-hours are obtained by multiplying the number of interrupted customers by the duration of the event. The sum of all customers-hours 498.33 is then divided by the total number of supplied customers 20000 to obtain a SAIDI value of 1.495 minutes for that particular day. The yearly SAIDI value is found by summing the daily values over one year.

- SAIFI: System Average Interruption Frequency Index. It represents, for a given area, the average frequency of interruptions per customer. This means how often a customer, on average, has lost power supply in one year (or a determined time). This is calculated by dividing the total number of interrupted customers by the total number of served customers. A SAIFI of 10 means that the customers connected to a power feeder experienced interruptions events in average 10 times in a year.
  For the previous example described in the SAIDI paragraph, the total number of interrupted customers is 555 for a total of served customers of 20000. This leads to a SAIFI of 555/20000 = 0.02775. That means that, on that particular day, the served customers at that utility have each a probability of 0.02775 of experiencing a power outage.
- CAIDI: Customer Average Interruption Duration Index. It is the average time for the service restoration to the average customer per sustained interruption. It is quite similar to the SAIDI except that the total customer-hours value is divided by the number of interrupted customers instead of the total number of the utility customers. Again from the above-mentioned example, the customers-hours are 498.33 and 555 customers were interrupted (Table 1-1). Therefore, the CAIDI is then 498.33/555 = 0.898 hour, this means 53.874 minutes. On average, each customer who experienced a power outage that particular day was out of service for 53.874 minutes.

Notice that the CAIDI can also be calculated by dividing the SAIDI by the SAIFI. With a SAIDI of 1.495 minutes and a SAIFI of 0.02775, CAIDI =1.495 minutes/ 0.02775 = 53.875 minutes.

Other less used indices are:

- CAIFI: Customer Average Interruption Frequency Index. Similar to the SAIFI, it gives the average number of interruptions per interrupted customer for a given period. It is simply the total number of interruptions divided by the total number of customers who experienced these interruptions.
  From the previous example, there were a total of 4 interruptions that affected 555 customers. So the CAIFI is 4/555= 0.0072.
- CIII: The Customer Interrupted per Interruption Index. This is the direct reciprocal of the CAIFI. It simply gives the average number of interrupted customers during one interruption event. It is the number of customers interrupted divided by the total number of occurred interruptions.
  The previous example shows that a total of 555 customers were affected by 4 interruptions. The CIII is 555/4=138.75. Each time there is an outage, an average of 138.75 customers is affected.
- ASAI: Average Service Availability Index. Also called the Service Reliability Index, it is the ratio of the total number of customer hours where the service was available to the

total customer hours demanded. It is generally calculated on a monthly or a yearly basis but can also be calculated for any period of time.
Still, from the given example in the SAIDI paragraph, the total customer-hours during the interruptions is 498.33. With a total number of customers of 20000 and considering only that particular day (the 15th day of the month), this means that the total demanded customers-hours is 20000 X 24 = 480000. The total customers-hours when the service was available is then the difference between the total demanded and the total interrupted customer-hours 480000-498.33= 479501.67. Then the ASAI is 479501.67/480000 this equals 99,896%.

Table 1-2: Example of ASAI Calculation

Date	Time	Interrupted Customers	Duration in minutes	Customers-hours
15th	08:20	100	90	150,00
15th	14:05	25	20	8,33
15th	14:50	400	45	300,00
15th	19:37	30	80	40,00
Sum		555	235	498,33
Total customers				20000
Total demanded customer-hours				480000
ASAI				99,896%

Knowing the SAIDI over a period of time T (day, month, year etc…), the ASAI can also be found as

$$ASAI = \left[\frac{(T - SAIDI)}{T}\right] \times 100 \qquad (1\text{-}1)$$

From our example with a SAIDI of 1.495 minutes for one day (24 hours), the ASAI is

$$ASAI = \left[\frac{24 - {}^{1.495}/_{60}}{24}\right] \times 100 = 99{,}896\% \qquad (1\text{-}2)$$

1.1.3 Reliability: the actual trends.

1.1.4 The limits of the Indices

The biggest drawback of this reliability metrics appears when it comes to comparing the reliability of different regions, cities or countries. These reliability indices are very sensitive to

- The local weather: it is well known that a big number of reliability problems nowadays are caused by the weather conditions. Therefore, a utility grid naturally confronted to a numerous lightning, tornadoes and strong winds may display worse reliability indices compared to a utility installed in a region with more clement weather conditions. Note that the weather condition also has an important impact on the vegetation growth that can also generate problems like trees falling on the utility equipment.

- The landscape and equipment accessibility: This plays an important role in the utility restoration time after an outage. The companies in charge of the utility maintenance would need more time to repair the failure if they have some difficulties to reach the damaged point. For example, bringing new pillar in a forest area with narrow roads in a mountain certainly requires a lot of time.
- The density of the customers: This parameter has a considerable effect on the length of distribution cable between the customers. Long distances between two connection points simply increase the probability to encounter problems on the way from one customer to the next. A utility providing energy to rural regions has somehow different concerns than that for a dense, crowded city. The rural region needs more equipment (transportation equipment) per customers served. This means that the probability that an equipment fails and causes an interruption increases. The large length of the distribution cables is also increasing the risks to have problems like birds and animals as well as fallen trees disturbing the utility.
- The utility design [3]: this criterion affects essentially the interruption time. After a fault, depending on the design, an alternative supply grid can be connected and continue feeding the customers while the fault is being repaired on the main supply. In a radial line design, which is usual in rural and remote regions, there is no alternative supply from the grid. This means, in case of an outage, that the customers have to wait until the utility crew has repaired the line. The ring design, offering a manual switch over the secondary supply by the crew, will considerably reduce the off voltage supply time experienced by the customers. This design is used mostly in urban regions with residential, commercial and light industrial sector. The last design type does not even let the customers notice that there was a fault (most of the time a brief voltage sag only can be noticed). This is the meshed design, which automatically switches to another supply source when its main source has a failure.

These are the reasons why the calculations are limited in the way they can be used. Even if the calculations methodologies may not change for different regions, the reliability indices are useful only for a particular region. However, for the same region, they represent very good measurements that can be used to observe and evaluate the extension and maintenance practices over the time.

1.2 Supply quality

Unlike the principle of reliability, which is easy to observe through the absence of light or the sudden stop of running machines and equipment caused by power supply interruption, the qualitative aspect is a characteristic that needs a higher level of observation or measurement technics and tools to be quantified. These two criteria are analogue to the product property concerning the food we eat. Considering an apple, the amount of apples produced and the effectiveness of its delivery service to the customers represents the reliability of the power supply. The number of nutrients and vitamins, as well as undesired heavy metal and chemical components contained in these apples, are compared to the quality of the power supply. Moreover, to be able to verify each quality criterion of the apples, more equipment than just the aspect and the weight are needed. It is similar to the power supply quality. The following

lines will develop the different qualitative problems of the supply power voltage, their sources and consequences and finally, how they are quantified.

1.2.1 Power Qualitative problems: indicators and measurement technics

In every country, the power supply voltage has special specifications that should be respected by the electrical power utility. The basics of them are the rated frequency and the rated amplitude. Any deviation from the perfect rated sinusoid shape will have an impact on the PQ. Transients, sag or under-voltage, swell or overvoltage, harmonic distortion, voltage fluctuations, frequency variation, unbalance, flicker and electric noise are the most common types of deviation from the rated voltage sinusoid shape. They have different sources that generate them and different impacts as well

1.2.1.1 Voltage Fluctuations

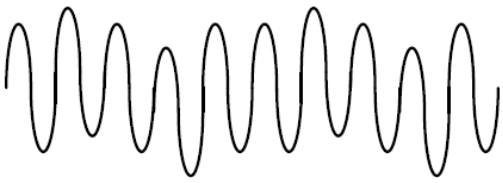


Figure 1-1: Voltage Waveform with Fluctuating Amplitude

The voltage fluctuation is a systematic or a random variation of the voltage value of which the magnitude remains in a certain limit. A systematic (periodic) fluctuation can be considered as the superposition of the normal sinusoidal voltage waveform and another sine wave with a much lower amplitude (up to 5% of the rated voltage) and a lower frequency of generally below 25 Hz [9]. The standard ANSI C84.-1982 defines the limits of fluctuations between minus to plus 10% of the rated voltage value and a classification is done depending on the type of the fluctuations [2] [10]. We can distinguish [2] :

- Step-voltage changes that can be regular or random in amplitude and in time.
- Cyclic voltage fluctuations or sinusoidal fluctuations that can be represented mathematically as an oscillating offset voltage added to the main voltage
- Random voltage fluctuations, which are just a random change in terms of timing (frequency) and amplitude.

Oscillating loads (fluctuating current drawl) can cause voltage fluctuations. The arc furnaces represent the most common equipment that generates voltage fluctuations [3]. Frequent starts and stops of rotating machines, like those of an elevator, cause also fluctuations [2]. The major consequences due to the voltage fluctuation are common to those of under-voltages like problems with the reactive power consumption and a noticeable instability of the internal voltage for electronic equipment. The most perceptible effect is flickering of incandescent lamps. They cause also the reduction of the performance of the equipment.

For each country, it exists a certain tolerance range of the voltage variation.

- The European countries tolerate variations from -10% to +10% of the rated voltage. The statistical evaluation is done on a dataset of one week of measurements. During 95% of that time, the fluctuations should not exceed the limits [10] [11].
- In South Africa, the rated supply voltage level for LV customers may be 400 V phase-to-phase and 230 V phase to neutral. Limits are set to ±15% for the rated voltage for

supplies voltages less than 500 V and ±10% for supplies voltages higher than 500 V [12].

- In Australia, the standard AS60038 requests that the voltage may vary only from -6% to +10% of the rated 230 V phase to neutral and 400V phase to phase voltage.
- Concerning the voltage variation in the USA, a distinction is made between the service voltage and the utilisation voltage. The service voltage is measured at the point of common coupling while the utilisation voltage is measured at the equipment using the electricity. The service voltage under normal operating conditions can vary in a range of ±5% of the rated supply voltage but in short duration or/and abnormal conditions, -8.33% to +5.83% is tolerated. On the customer side, the utilisation voltage under normal conditions can reach a maximum of 5% of a standard voltage greater than 600 V, if the rated voltage is less than 600 V, the maximum limit decreases to 4.17%. The lower limit in both cases (voltage greater or less than 600 V) is -8.33%. A further exception is made, reducing to -10% the lower limit if the circuits do not contain lighting equipment. When the utility system is operating in contingency conditions, the upper limit of the utilisation voltage is +5.83% and the lower one is -11.67% of the rated voltage for both rated voltage levels (greater or lower than 600 V). The lower limit can be -13.33% if the circuit contains no lighting equipment [13].

1.2.1.2 Frequency Variations

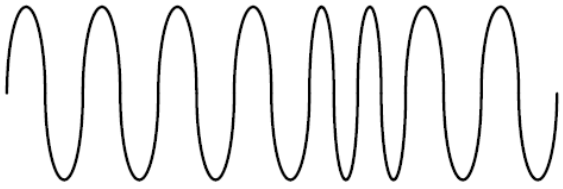


Figure 1-2: Voltage Waveform with Constant Magnitude but Fluctuating Frequency

The power frequency variation is the deviation of the power system fundamental frequency from its defined rated value that can be 50 Hz like in Europe or 60 Hz in the US for instance. This is a really rare voltage disturbance especially for an interconnected power system [9]. The frequency variations are mainly caused by the difference between the active power demand and the power generated [2]. In off-grid sites where a dedicated generator is installed, generally with poor power infrastructure, frequency variations are more common in case of overloaded generator [9]. In an interconnected situation, separated generators are all synchronised at a common frequency and are controlled to remain at that frequency. Any heavy load change (turn on or off) that would normally have a noticeable impact if it were fed only by one generation, will have a barely noticeable impact on the frequency. This is because the impact of the step change in terms of frequency as well as of voltage magnitude is divided among all the connected generators. Each generator will then notice only a very small variation and the regulation system will consequently need a very short time to get back to the set points values.

In general, ICT equipment tolerate quite well small frequency fluctuations. More impacted by frequency variations are devices relying on a constant cycling of power over time like motors. The frequency determines the rotation speed of the motors so any change can make it run faster or slower. This would probably lead to a less efficient operating point of the motor. This

can cause extra heat and increase the degradation rate of the motor elements through the additional current draw.

The frequency of the supply voltage, despite its relatively good stability, has some defined limits recommendations.

- In Europe, the EN50160 standard sets a compliance limit of ±1% of the rated 50Hz frequency during 95% of the time in one week and +4% to -6% of the rated frequency during 100% of the time in one week [11].
- The South African standard NRS 048-2 sets different limits depending on the network type. For the national grid, the required limit is ±2.5% of 50 Hz the standard frequency and for island networks, off-grid, and the limits are extended to ±5%. The measurements should be done during one year and the frequency deviation during 99.5% for grid networks and 95% for island network shall meet the requirements [4].
- 50 Hz is also the standard frequency in Australia and the variation limits in a good operating mode may vary between 49.75 and 50.25 Hz, this is ±0.5% of the rated frequency. Depending on some contingency that can happen on the network, these limits can reach ±6% for example in the case of multiple contingencies happening on the grid [3].
- The US standard frequency is set at 60 Hz. Under continuous operation, this can have a variation of ±2% whereas the lower and upper limits are -5% and +3% respectively for a temporary contingency operation with reduced performance [14].

1.2.1.3 Unbalance

In a three-phase system, it can happen that the three voltage magnitudes are not equal and/or the angles (phase difference) between them are not exactly 120 degrees. This is called voltage unbalance. When this voltage supply disturbance occurs, the cause is generally not on the utility side but on the customer side. It is mainly caused by facility loads [3] [15]. The most common system configuration leading to a voltage unbalance is the unequal single-phase load distribution [3]. Most of the electrical appliances and equipment in the houses and in the industry are single-phase but the utility supply is a 3-phase. The loads can then be connected to one single phase. If the load among different phases is not equally distributed, the parameters of each microsystem (made up of each single phase as supply and its connected loads) will differ from the others and this will cause an unbalanced power demand. The voltage unbalance can also appear when there is no transposition of the transmission lines. The transposition is a measure to equalize the impedance relative to the ground of each phase. The main consequence of an unbalanced power system is the impact on the system stability by causing supplementary drawl of reactive power. The malfunction of some equipment, as well as measurements and control devices, can also result from unbalance. Especially in the case of a motor (the most affected load by unbalance), big unbalance may cause extra heat generation in the motor components and so reduces its lifetime [16] [17].

There exist some calculation methodologies to evaluate the degree of unbalance of a system.

One method, defined by the NEMA (National Electrical Manufacturers Association in the USA) and also used in the IEEE community [18], is to calculate the maximum deviation from the average voltage value of the 3-phase voltages. Then the maximum deviation is divided by the

average value previously mentioned. The NEMA definition uses the line voltage and is known as the Line Voltage Unbalance Rate (LVUR) whereas the IEEE uses the phase voltage and this is known as the Phase voltage Unbalance Rate (PVUR) [18].

$$\%LVUR = \frac{\max voltage\ deviation\ to\ the\ average\ line\ voltage}{average\ line\ voltage} \times 100 \qquad (1\text{-}3)$$

$$\%PVUR = \frac{\max voltage\ deviation\ to\ the\ average\ phase\ voltage}{average\ phase\ voltage} \times 100 \qquad (1\text{-}4)$$

Let us consider a 3-phase system with the lines voltages values 230, 220 and 222 on the lines A, B and C respectively. The value of the arithmetic average of the line voltage is then 224. The largest deviation from the average 6V (230V-224V) is on the line A. Then the degree of unbalance %LVUR is 6V/224V, i.e. 2.68%.

The true calculation of the voltage unbalance method consists of computing the ratio of the negative or zero sequence component to the positive component. This defined the DQV2 unbalance index expressed in percent. In a 3 phase system A, B, C and N where N represents the neutral conductor,

$$DQV_2 = \frac{|V_{an2}|}{|V_{an1}|} \times 100 = \frac{|V_{ab2}|}{|V_{ab1}|} \times 100 \qquad (1\text{-}5)$$

With V_{an1} representing the positive and V_{an2} the negative sequence phase-to-ground voltages. Respectively, V_{ab1} and V_{ab2} are the positive and negative sequence of the phase-to-phase voltages. The resulting value can be expressed in percentage if multiplied by 100. The complexity of this method is the calculation of the positive and negative sequences that requires the measurement of not only the magnitudes but also the phase (angular position) of each voltage signal.

$$V_{ab1} = \frac{V_{ab} + a\,V_{bc} + a^2 V_{ca}}{3}$$
$$V_{ab2} = \frac{V_{ab} + a^2 V_{bc} + a V_{ca}}{3} \qquad (1\text{-}6)$$
$$With\ a = -\frac{1}{2} + j\frac{\sqrt{3}}{2}\ and\ a^2 = -\frac{1}{2} - j\frac{\sqrt{3}}{2}$$

Example: first, let's consider the ideal system with a voltage magnitude value of 400V between each line and the phases 0, -120° and +120° between line a and b, b and c and c and a respectively. Writing the voltages in the complex forms leads to:

$$V_{ab1} = \frac{1}{3} \times 400V \cdot \begin{bmatrix} 1 & -\frac{1}{2} - j\frac{\sqrt{3}}{2} & -\frac{1}{2} + j\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} 1 \\ -\frac{1}{2} + j\frac{\sqrt{3}}{2} \\ -\frac{1}{2} - j\frac{\sqrt{3}}{2} \end{bmatrix}$$

$$V_{ab1} = \frac{1}{3} \times 400V \times 3 = 400V$$

$$V_{ab2} = \frac{1}{3} \times 400V \cdot \begin{bmatrix} 1 & -\frac{1}{2} - j\frac{\sqrt{3}}{2} & -\frac{1}{2} + j\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} 1 \\ -\frac{1}{2} - j\frac{\sqrt{3}}{2} \\ -\frac{1}{2} + j\frac{\sqrt{3}}{2} \end{bmatrix}$$

$$V_{ab2} = \frac{1}{3} \times 400V \times 0 = 0$$

So the degree of unbalance is equal to:

$$\%unbalance = \frac{0}{400} \times 100 = 0\%.$$

This is exactly the expected value for the perfect network configuration.

Now let us do the same calculation for another configuration described as follows:

$$\begin{cases} V_{ab} = 390V, \varphi_{ab} = 0° \\ V_{bc} = 420V, \varphi_{bc} = -122° \\ V_{bc} = 370V, \varphi_{bc} = +130° \end{cases}$$

Rewriting these values into the complex form gives

$$\begin{cases} V_{ab} = 390V\ (\cos(0°) + j \cdot \sin(0°)) \\ V_{bc} = 420V\ (\cos(-122°) + j \cdot \sin(-122°)) \\ V_{bc} = 370\ V\ (\cos(130°) + j \cdot \sin(130°)) \end{cases} \rightarrow \begin{cases} V_{ab} = 390V \\ V_{bc} = 222.57V - 356.18\ V \cdot j \\ V_{ca} = -237.83V + 283.44V \cdot j \end{cases}$$

$$V_{ab1} = \frac{1}{3} \cdot [390 \quad 222.57 - 356.18\,j \quad -252.34 + 270.60j] \cdot \begin{bmatrix} 1 \\ -\frac{1}{2} + j\frac{\sqrt{3}}{2} \\ -\frac{1}{2} - j\frac{\sqrt{3}}{2} \end{bmatrix} \text{(in V)}$$

$$V_{ab1} = 390.01 + 22.85\,j(\text{in V}) \rightarrow V_{ab1} = 390.75V\ (\cos(3.35°) + j\sin(3.35°)) = 390.75V\ \angle 3.35°$$

$$V_{ab2} = \frac{1}{3} \cdot [390 \quad 222.57 - 356.18\,j \quad -237.83 + 283.44\,j] \cdot \begin{bmatrix} 1 \\ -\frac{1}{2} - j\frac{\sqrt{3}}{2} \\ -\frac{1}{2} + j\frac{\sqrt{3}}{2} \end{bmatrix} \text{(in V)}$$

$$V_{ab2} = 28.21 + 5.66\,j(\text{in V}) \rightarrow V_{ab2} = 28.77V(\cos(11.35°) + j\sin(11.35°)) = 28.77\ V\angle 11.35°$$

The unbalance degree %unbalance is then

$$\%unbalance = \frac{28.77}{390.75} \times 100 = 7.36\%.$$

To avoid the complex algebra calculations, involving the amplitudes and the angles of the voltages, the following formula gives a very good approximation of the true definition [18]. The simplified unbalance rate %unbalance$_s$ is

$$\%unbalance_s\ [\%] = \frac{82 \cdot \sqrt{(V_{ab} - V_{avg})^2 + (V_{bc} - V_{avg})^2 + (V_{ca} - V_{avg})^2}}{V_{avg}} \qquad (1\text{-}7)$$

Where V_{avg} represents the average line voltage.

Applying this formula to the previously described unbalanced system, the average value is 393.33V. This leads to

$$\%unbalance_s\ [\%] = \frac{82 \cdot \sqrt{(390-393.33)^2 + (420-393.33)^2 + (370-393.33)^2}}{393.33}$$

$$\%unbalance_s\ [\%] = \frac{2918.4}{393.33} = 7.41\%$$

The NEMA method gives a maximum deviation to the average 393.33V of 26.67V (420V-393.33V). This corresponds to an unbalance degree of $\frac{26.67}{393.33} \times 100 = 6.78\%$.

It appears that the simplified formula approximates well the definition formula without complex calculations. This can be useful for embedded systems where the computational resources are limited and the control algorithms are very time-critical. The NEMA method is again more simplified. The results are losing some accuracy. This method can be used to get a quick overview of the system quality especially in case there is no mean for complicated operations.

Another simplified method called CIGRE-2 [19] that presents some similarities with the simplified version of the true definition, gives the unbalance degree as follows:

$$\%unbalance_C\ [\%] = \frac{\sqrt{2/3\left[\left(V_{ab}-V_{avg}\right)^2 + \left(V_{bc}-V_{avg}\right)^2 + \left(V_{ca}-V_{avg}\right)^2\right]}}{V_{avg}} \times 100 \qquad (1\text{-}8)$$

This delivers for the same example as before, an unbalance degree of 7.39%.

Depending on the region or countries, the limits and even the calculation of the degree of unbalance can differ.

- The European Standard EN50160 uses the true definition calculation and the obtained unbalance rate of the system should be less than 2%. The measurements and calculation have a sampling rate of 10 min during one week. 95% of the time during that week, the unbalance rate has to be less than 2% [10] [11].
- The South African standard NRS-048 described the unbalance rate UB using the zero and negative sequence voltages. The limitation is also fixed at maximum 2% but in networks with a predominance of single or two phase customers, the maximum unbalance level can be increased to 3% [4].
- The Australian standard is similar to the calculation method and the target maximum value as the EN50160: The maximum unbalance degree is 2% [3].
- The US standard ANSI C84.1 uses the NEMA definition for the unbalance rate calculation and recommends the limit of 3% [13] [20].

1.2.1.4 Sag and Under-voltage

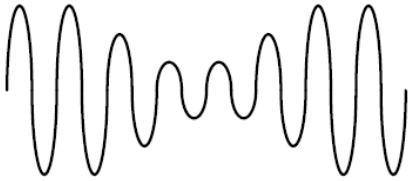


Figure 1-3: Voltage Waveform Before, During and After a Sag

Also called a voltage dip, a sag is a short (quick) reduction of the voltage level from 90% to 10% of the rated voltage value. They can last between a half cycle and one minute [2]. The IEEE 1159 document gives a further classification into three groups depending on the duration. Instantaneous sags last between 0.5 and 30 cycles; momentary from 0.5 to 3 seconds and the temporary ones have a duration from 3 seconds up to 1 minute [21]. During this time, the remaining voltage wave remains at the same frequency. Sags can be caused by:

- Energizing heavy loads: the sudden energising of heavy loads like arc furnace automatically reduces the voltage. If the power supply is able to deliver the supplementary required energy, then the voltage level will quickly come back to its rated value [2] [15].
- Starting a large motor: A motor can need very high current while starting, up to 5 times its nominal current. This big current withdrawal can likely cause a considerable voltage drop [9] [21].
- Fault on the transmission network: especially the case for parallel feeders, if there is a fault on one power feeder, a sag will be noticed until the regulation system corrects it either by switching on another feeder or by increasing the power output of the remaining, still working, feeders [15] [3].

As the voltage level of a sag is below the rated level, the impact is non-destructive but has more to do with the stability and control of the system. They can cause for instance the malfunction of an ICT equipment like PLCs, PCs and control equipment based on microprocessors that can lead to a process stop. For rotating machines, it induces a reduction of the efficiency [2] [15].

An under-voltage is simply a long sag over more than one minute. The causes are similar to those of a sag but sustained [2]. These causes are

- Overload: when the power supply is not able to provide the requested power.
- Less supply capability or sustained fault: a sudden reduction of the supply capacity to keep feeding the connected loads. The main consequences of the under-voltage are instability, high reactive power demand and high current draw in motors.

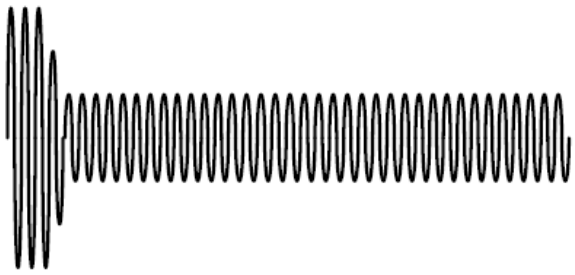


Figure 1-4: Voltage Waveform Before and During an Under-voltage

The reduction of the number of sags and their severity is strongly related to the improvement made on the network to minimise the faults. The line shielding, for instance, is helpful to prevent lightning. A regular cleaning plan around the distribution lines avoids that trees fall on the cables. On the customer side, an essential measure to avoid the voltages sags is to choose carefully the equipment. By purchasing expensive and sensitive equipment, the customer has to make sure that it can cope with reasonable sags to a certain level without damage or malfunction. Besides, there are actually certain practices used by the customers to reduce the potential problems linked to the voltage sags [22]:

- Correct connection to the ground
- Good wiring: for example, if the lights are on the same panel as a motor like an elevator's motor, the light will surely blink every time the motor starts: when the elevator is called
- Use of a sag mitigation equipment [22]: Customers experiencing severe equipment dysfunction due to the voltage sags might consider installing one sag mitigation equipment. This equipment can be:
    - An Uninterruptible Power Supply (UPS)
    - Ride-Through Capacitors: in case of power loss or reduction, they provide for few seconds the necessary voltage to the system.
    - Ferro resonant or Constant Voltage Transformer (CVT): having enough energy stored in the transformer core when saturated, it provides the little energy needed to compensate the voltage dips.

1.2.1.5 Swell and overvoltage

The swell is a momentary increase of the voltage, i.e. the inverse of a sag. The IEEE 1159-1995 Recommended Practice on Monitoring Electric Power Quality defines it as an increase of the voltage magnitude in ranges from 10% to 80% above the rated value and happens at the same power frequency for a duration between half a cycle and one minute.

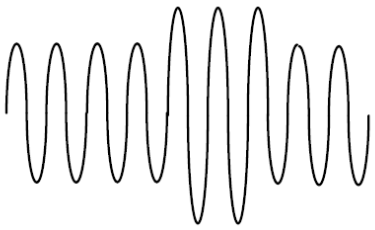


Figure 1-5: Voltage Waveform Before, During and After a Swell

Like the sags, the swells can also be divided into 3 categories: the instantaneous swell with a duration of 0.5 to 30 cycles, the momentary one that lasts between 0.5 and 3 seconds and the temporary one with a duration from 3 up to 60 seconds. Generally, the voltage swells are less common than the voltage sags and are mainly caused by switching off heavy loads: an abrupt reduction of large power consuming loads by switching them off generates a large voltage swell in the system according to the formula $\mathrm{v} = \mathrm{L}\frac{\mathrm{di}}{\mathrm{dt}}$. Where L is the inductance as the load is supposed to be inductive and di/dt is the derivative of the current over the time. A swell can occur due to a single line-to-ground fault on the system, which can also result in a temporary voltage rise on the unfaulty phases. This is especially true in ungrounded or floating ground

delta systems, where the sudden change in ground reference results in a voltage rise on the ungrounded phases. Energizing a capacitor bank can also cause a swell even though the more common effect is an oscillatory transient [21]. The effects of swells are potentially more damaging than those of sags. They may affect the stability of the voltage regulation, interface with communication signals, cause the malfunction of measuring and control equipment as well uninterruptible power supply (UPS) [2].

The overvoltage is to the swell what the under-voltage is to the §§sag: an extension in time of a swell. Once a swell duration exceeds 1 minute, it is called an overvoltage.

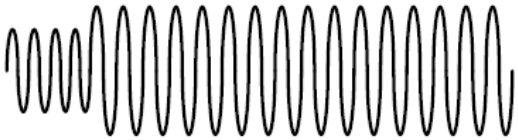


Figure 1-6: Voltage Waveform Before and During an Overvoltage

The main causes of the overvoltage in the power grids are [2] :

- The incorrect setup of a supply transformer tap: this is quite common when the inhabitants of a given region reduce the power usage during summer while the transformer is still set for a much higher power output.
- The lightning
- The load switching: The events like the opening of protection devices or the switching on and off of a capacitive circuit, causes a rapid change of the network structure that can produce an overvoltage.

The impacts of the overvoltage can be for instance an additional stress on the insulation materials in the electrical machines and a voltage instability [2]. At an overvoltage event, the flowing current can get higher leading to the tripping of circuit breakers. The overcurrent increases the losses and can easily generate an overheating of the equipment. This is a big concern for example for the ICT enterprises with big data centers that need really efficient cooling systems.

Most of the voltage sags and swells events are caused by faults on the distribution systems or the switching on and off of loads and also the under and overvoltage are essentially generated by the faults on the utility system. These network faults may essentially be caused by environmental events like accidents, birds, equipment failures, wind and lightning. Even though they have impacts on the shape of the supply voltage, the quality of the supply, they are more related to the power reliability. In spite of all the prevention and the precautions applied, it is almost impossible to have a complete disturbance-free utility. The level and the number of disturbances occurring per year are strongly depending on the location. Lightning protection can be installed but it is hard to determine where it should be mounted. It is not possible to choose which ways the birds should fly or what should be the maximum wind speed. That is why it is impossible for any regulation system to define an index or a reference/rated value concerning the level the frequency and the number of these disturbances over a given period. The essential objective is then to minimise their impact by

improving the distribution system in terms of fault detection and recovery, lightning protection, structural stability etc.

Nevertheless, there are some indicative values concerning the number of occurrences. For example, in Europe, one can count one thousand voltage sags in average per year. In South-Africa, the number of voltage sags occurring over one year can reach 2200 and 75% of them happens on the rural network. About 50% of them are momentary sags (duration between 0.5 and 3 seconds) [4]. Across North America, they are about 1600 occurrences per year with 60% lasting less than 10 ms (instantaneous sags) [22].

1.2.1.6 Transients

The transients qualify a phenomenon or a quantity that varies from one steady state to another during a very short time period compared to the whole time duration of the observed phenomenon or quantity [23]. In the power systems, the transients can be seen in the voltage: a very high and quick rise of the voltage over a very short time – impulsive [9]. They can also appear as a damped oscillatory wave with a very high first voltage peak – oscillatory [9]. They may reach five to ten times the level of the rated voltage and therefore are probably the least present but the most dangerous disturbance of the power systems.

- The impulsive transients also referred to as surge, glitch or spikes, can be further distinguished in function of their speed. However, there is no defined time limit of a transient. Most of the time, an event of which duration is less than one cycle is considered as transient. They can also be extremely fast, rising to the peak in 5 nanoseconds to completely fall to zero in less than 45 nanoseconds.

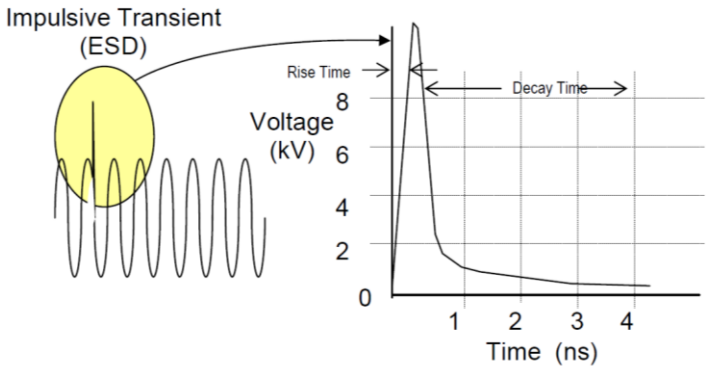


Figure 1-7: Voltage Distortion and Duration of an Impulsive Transient

They are quickly damped by the resistive elements of the circuit and therefore do not propagate far away from their source. The effects are much localized.
The impulsive transients are essentially caused by the lightning. An impulsive overvoltage appears after a lightning strike hitting a transmission line (direct stroke). This can also be induced by nearby strokes to the ground or in the clouds.

- Oscillatory transients are alternating by nature. The high voltage level variation appears as a damped oscillation with a frequency of some hundred Hertz to some Megahertz. It causes the power signal to alternately swell and then decay very quickly (a decaying oscillation).

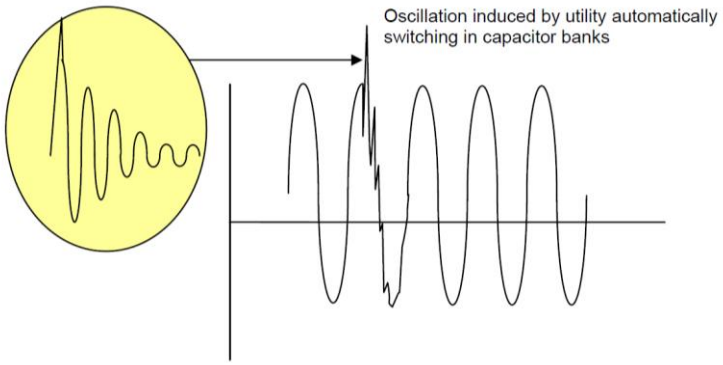


Figure 1-8: Voltage Distortion Caused by an Oscillatory Transient

Inherently, any system always presents a certain resistance to change from a stable steady state. Therefore, oscillatory transients can be considered as the reaction against the state change of the electrical system. They are caused by the energizing of capacitive or inductive loads such as a capacitor bank or a motor [9]. They can also happen when a power transmission line is energized. The frequency of the oscillation is defined by the reactance of the energized electrical component (capacitor bank or transmission line) and the inductance of the feeding circuit.

Independently of the transient originator events, the effects of the transients are strongly related to the operational performance of the measuring and protective system. They negatively interfere with the correct operation of the circuit breakers and can cause malfunction of the relays. High transients can even destroy the equipment and the insulation materials. The ICT (the electronic) are the most sensitive to the transients because even non-material-damaging transients can still lead to some serious disruption due to data corruption or loss.

1.2.1.7 Harmonics

Unlike the voltage disturbances like the transients, the voltage sags or swell that last only for a very short period, the harmonics are steady-state phenomena that cause a continuous distortion of the fundamental current and voltage waveforms. The harmonics are oscillating voltages, different from the fundamental rated voltage signal and of which frequencies are multiples of that of the main voltage. They are superimposed to the fundamental and it finally results in a nonsinusoidal waveform.

Figure 1-9: Voltage Distorted by Harmonics

Depending on the ratio of the harmonic frequency to the fundamental frequency, it can be distinguished [2]:

- The even harmonics: These are integer harmonics having frequencies even integer multiple (2, 4, 6…) of the fundamental frequency.

- The odd harmonics: When the harmonics frequencies have frequencies, which are odd integer multiple (3, 5, 7…) of the fundamental frequency, they are called odd harmonics.
- Sub-harmonics: in this case, the harmonic frequencies are less than that of the fundamental.

Inter-harmonics: if the harmonics frequencies are fractional multiple but greater than the fundamental frequency (1.2, 1.5, 3.7…), they are known as inter-harmonics.

Generally, harmonics are produced by non-linear loads that absorb non-sinusoidal currents and these non-sinusoidal currents cause a distortion of the original voltage waveform as a feedback effect due to the internal impedance of the voltage source like for instance a transformer. They are characterized by the fact that the waveforms of the circulating current are not purely sinusoidal, even if they are fed by a perfect sinusoidal voltage. A distinction can be made between two groups of non-linear loads: The “modern” non-linear loads including energy converters based on power electronic components and the “classical” non-linear loads not related to the power electronics but, for instance, to:

- Transformers
- Rotating machines
- Fluorescent lamps with magnetic ballasts
- Arc furnaces
- Welding machines

Already in use for many decades, these loads rely on the magnetization hysteresis effect where they operate near the knee of the saturation curve of the material (of which the magnetic characteristic is not linear). There are also arcing devices; their operating voltage-current characteristics are extremely non-linear as shown in Figure 1-10.

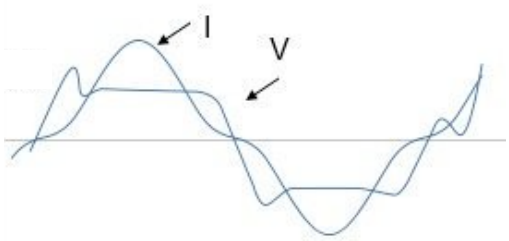


Figure 1-10: Typical Voltage and Current Waveform for Arc Furnaces

“Modern” non-linear loads are for example:

- Inverter-fed AC voltage sources
- Adjustable speed drives (ASD) (Figure 1-11)
- Energy-efficient lighting (Figure 1-12 [24])
- DC converters

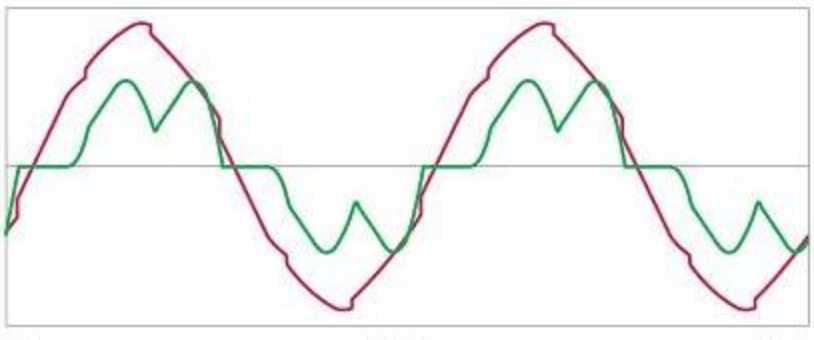


Figure 1-11: Typical Voltage and Current Waveform for a VSI-based Variable Speed Drive

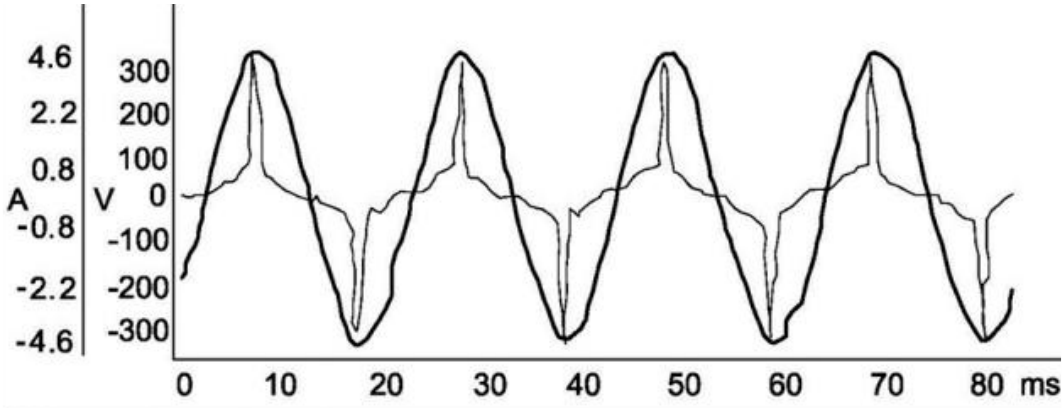


Figure 1-12: Typical Voltage and Current Waveform for LED Lighting Bulbs

Such equipment is based on semiconductors devices like diodes, IGBT's, GTO's. The different generated harmonics (frequency and magnitude) depend on the topology, design and operating principle of the switching circuits. For example, a 6-pulse rectifier will cause harmonics at the 5^{th}, 7^{th}, 11^{th}, 13^{th}, etc. order. In this case, the magnitude of each harmonic is inversely proportional to the harmonic order. The one generated by a 12 pulse rectifier are the 11^{th}, 13^{th}, 23th, 25^{th}, etc. with magnitudes of about 10 percent of those for the 6-pulse rectifier [25]. Generally, line-commutated devices (such as the ones mentioned before) will also have harmonic characteristics different from those of forced commutation devices (such as PWM converters)

The major effects generated by the harmonics are the resonance, the increase of the RMS voltage and current values and excessive neutral currents [26]. These may have direct consequences as:

- Overheating of equipment and grid components,
- Malfunction of circuit breakers,
- Capacitor damage,
- Malfunction or damage of sensitive electronic equipment,
- Motor shaft torque oscillations,
- Equipment lifetime shortening,
- Noise in communication signals.

On a second level, once an equipment is damaged, a part of the whole power supply can be interrupted and most of the time, only at this stage, the harmonics distortion problem is detected.

The economic impact due to these material-related effects, which can lead to power outages, is very large. The digital economy (data storage, retrieval and processing), the continuous process manufacturing (paper, oil, clay, steel, glass) and the manufacturing & essential services (railroads, wastewater treatment) are the three sectors most sensitive to the power quality problems [27]. In the USA, already the power quality disturbances only are the cause of 6.7 billion dollars losses every year [27]. A survey realized by the Electric Power Research Institute (EPRI) reveals that the harmonics are the source of 22% of all the power disturbances [28].

The level of the waveform degradation caused by harmonics is generally represented by the THD (total harmonic distortion), which corresponds to the ratio of the RMS value of the harmonic content of the original signal to the RMS value of the fundamental of the original signal. Computable for the voltage or/and the current, it is expressed as a percentage of the fundamental and is calculated as follows:

$$THD = \sqrt{\frac{sum\ of\ squares\ of\ amplitudes\ of\ all\ harmonics}{square\ of\ amplitude\ of\ the\ fundamental}} \times 100\% \quad (1\text{-}9)$$

$$THD_V = \sqrt{\frac{V_1^2 + V_2^2 + V_3^2 + V_4^2 + \cdots + V_n^2}{V_1^2}} \times 100\% \quad (1\text{-}10)$$

Where n represents the order of the harmonic therefore V_n the amplitude of the harmonic of the order n and V_1 is the amplitude of the fundamental voltage.

The harmonic content of the grid voltage is also well standardised all over the world.

1. The European standard EN50160 [29] sets a general limit of the THD at 8% including all harmonics up to the 40th order. Moreover, each individual harmonic should be less than the value given in Table 1-3. These RMS values are calculated over one week with 10 minutes time interval and these constraints shall be met during 95% of the time. It can be noticed that there is no value for harmonics of order higher than 25. The reason for this is that they are not only usually very small but also very unpredictable due to resonance effects.

Table 1-3: European Standard Recommended Individuals Harmonics Values

Odd harmonics				Even harmonics	
Not multiples of 3		Multiples of 3			
Order h	Relative voltage (U_n)	Order h	Relative voltage (U_n)	Order h	Relative voltage (U_n)
5	6,0 %	3	5,0 %	2	2,0 %
7	5,0 %	9	1,5 %	4	1,0 %
11	3,5 %	15	0,5 %	6 … 24	0,5 %
13	3,0 %	21	0,5 %		
17	2,0 %				
19	1,5 %				
23	1,5 %				
25	1,5 %				

2. The South African compliance [12] for the low and medium voltage power systems are similar to the EN50160 standard concerning the THD as well as the individual

harmonics up to the 17th order. The Table 1-4 presents the limits set for individual harmonics. Unlike the European standard, there exist generic formulas to determine the limits for the harmonics of orders greater than 17, 21, and 10 for odd integer not multiple of 3, integer multiple of 3 and integer even harmonics respectively.

Table 1-4: South African Standard Recommendation for Individual Harmonics Values

1	2	3	4	5	6
Odd harmonics				**Even harmonics**	
Not multiples of 3		**Multiples of 3** (See note)			
Order *h*	**magnitude** %	**Order** *h*	**magnitude** %	**Order** *h*	**magnitude** %
5	6	3	5	2	2
7	5	9	1,5	4	1
11	3,5	15	0,5	6	0,5
13	3	21	0,3	8	0,5
$17 \leq h \leq 49$	{2,27 x (17/*h*)} – 0,27	$21 \leq h \leq 45$	0,2	$10 \leq h \leq 50$	{0,25 x (10/*h*)} + 0,25

The assessment period should be at least seven consecutive days (one week). As for the EN50160, the RMS value is computed every 10 minutes and these limits should be respected 95% of the time.

3. The maximum THD for the Australian standard is also set at 8% with the assessment period as the previous standards. Exceptions are made by defining the individual harmonics limits depicted in Table 1-5 [30].

Table 1-5: Australian Standard Recommendation for Individual Harmonics Values

Odd harmonics Non-multiples of 3		Odd harmonics Multiples of 3 (triplens)		Even harmonics	
Order, h	% harmonic voltage	Order, h	% harmonic voltage	Order, h	%harmonic voltage
5	5	3	5	2	2
7	5	9	1.5	4	1
11	3.5	15	0.3	6	0.5
13	3	21	0.2	8	0.5
17	2	>21	0.2	10	0.5
19	1.5			12	0.2
23	1.5			>12	0.2
25	1.5				
>25	0.2 + 1.1(25/h)				

4. The IEEE 519 standard in the US set the individual harmonics limits to 3% while the maximum THD is 5% [13]. Moreover, the IEEE519 standard is more concerned by the TDD (total demand distortion), which corresponds to the ratio of the harmonic current distortion to the maximum demand load current. The TDD is similar to the THD except that the maximum demand current (measured over 15 or 30 minutes) is used instead of the fundamental current.

$$TDD = \sqrt{\frac{I_1^2 + I_2^2 + I_3^2 + I_4^2 + \cdots + I_n^2}{I_{Lmax}^2}} \times 100\% \qquad (1\text{-}11)$$

The maximum values of the harmonic current distortion are given in Table 1-6 for a service voltage lower than or equal to 69kV.

Table 1-6: US Standard Harmonic Current Distortion Limits for Service Voltage below 69kV

SCR= I_{SC}/I_L	h<11	11≤h<17	17≤h<23	23 ≤h< 35	35 ≤h	TDD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.0	4.5	4.0	1.5	0.7	12.0
100-1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

SCR is the short circuit ratio.

I_{SC} is the short circuit current.

I_L is the customer average demand current.

h represents the harmonic number.

The very interesting aspect contained in the TDD is that it represents the evaluation of the consequences caused by the distorted current. Focusing only on the current THD could be misleading, because a small current can have a high THD but no significant threat for the main supply voltage, therefore no impact on the surrounding electrical devices. For example, many adjustable speed drives exhibit very high THD values for the current but are operating at very light loads, therefore very low current magnitude. This could be neglected since the level of the low current flowing has nearly no impact on the supply voltage.

2 Harmonics Filtering in the Power Systems - State of the Art

Harmonics filtering has progressively become a standard measure of the power quality improvement. As the knowledge of the impact of harmonics, such as overheating and fast ageing, was increasing, different measures have been taken in order to fix the issue. The first measures are preventive measures that focus on minimizing the harmonics production into the power system. Such measures could strongly apply the standard, in such a way like for instance the use of twelve-pulse converters instead of six-pulse ones. The IEEE 519 "Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems" introduced the total demand distortion TDD that is a maximum limit of harmonic distortion a customer is allowed to generate. The remedial measures consist of installing designed harmonics filters in the system that absorb the eventual harmonics currents or voltages. These curative appliances can be divided into passive harmonics filters and active harmonic filters. In general, they are installed on the load side, very close to the harmonic source. This chapter focuses on the remedial measures against harmonics in the power grid. A particular attention is given to the new trend in active power filters as they have experienced the biggest progress in the last three decades.

2.1 Passive Harmonic Filters

Passive filters are electrical circuits composed of basic passive electrical components elements that are capacitors, inductors and resistors. Traditionally used for the harmonics mitigation in power lines due to their simplicity, their technology has considerably evolved over the years. However, they are still widely applied especially in the transmission and distribution power grids as they can be used also as pure reactive power compensators [31]. The basic configuration of the passive filter integrated to the power supply shown in Figure 2-1. Usually branched as shunt element in parallel to the load, they can also be connected in series with the load [32]. The main advantage of shunt passive filters compared to series ones is their reduced rating power as only a fraction of the whole system current flows through. The passive filter elements are combined in such a way that they don't impact the fundamental frequency voltage of the grid (high impedance) but naturally absorb the maximum of the targeted harmonics power (low impedance) leading in consuming the most part of the harmonic currents generated by the load.

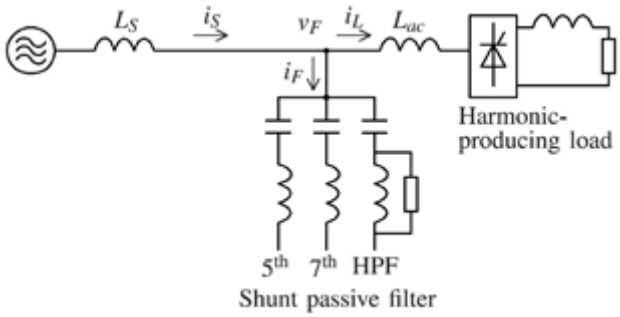


Figure 2-1: Typical Configuration of Passive Shunt Filter

The passive filter circuits can be classified into tuned filters and high-pass filters as depicted in Figure 2-3 and Figure 2-4. Single tuned filters are the simplest and therefore the cheapest harmonic filter compared to any other filter [33]. They are designed to mitigate a specific harmonic frequency and therefore can be considered as a band-stop voltage filter whereas

double tuned filters can mitigate two distinct harmonics frequencies but require more components compared to two single-tuned filters. The tuned filters circuits are designed so that they resonate at the same frequency as the harmonic to be filtered. The performance of tuned filters is evaluated by the quality factor Q of the filter that indicates how narrow the bandwidth of the filter is. Based on the filter characteristic depicted in Figure 2-2, the quality factor Q is calculated as follows:

$$Q = \frac{f_c}{f_2 - f_1} \qquad (2\text{-}1)$$

Where:

f_c: is the frequency with the highest gain (filter's rated frequency)

f_1 and f_2: the frequency bandwidth lower and upper limits at -3dB

Q is also related to the energetic performance of the filter as it is related to the inherent losses.

$$Q = 2\pi f_c \times \frac{energy\ stored}{energy\ losses\ per\ cycle} \qquad (2\text{-}2)$$

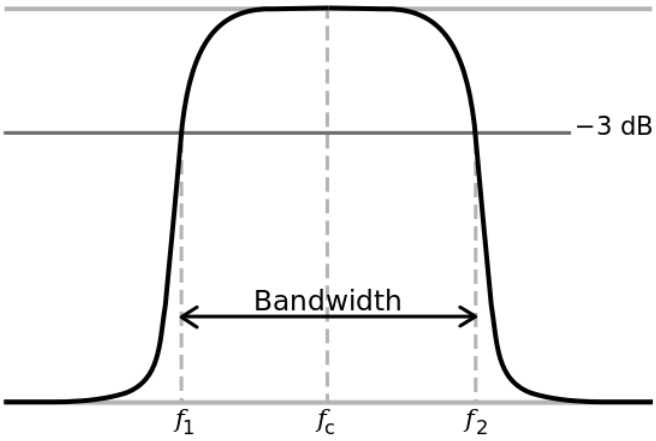


Figure 2-2: Example of the Frequency Response of a Tuned Band-pass Filter

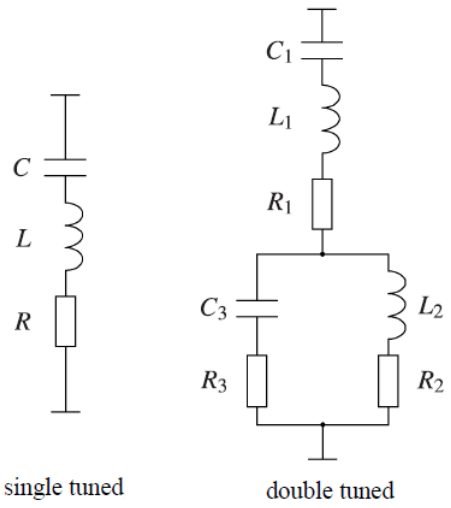


Figure 2-3: Typical Passive Tuned Filters

Therefore, the design of tuned filters circuits aims at maximizing the value of Q with the minimum possible components. Usually, the value of Q varies from 20 to 100 [34]. The higher Q, the sharper the peak and the lower the losses and therefore the more efficient the circuit.

The high-pass passive filters are different from the tuned ones because they are designed to mitigate a range of harmonic frequencies. They are thus cheap, easy to design and also reliable, even though they do not achieve the same filtering efficiency for all the filtered harmonic frequencies.

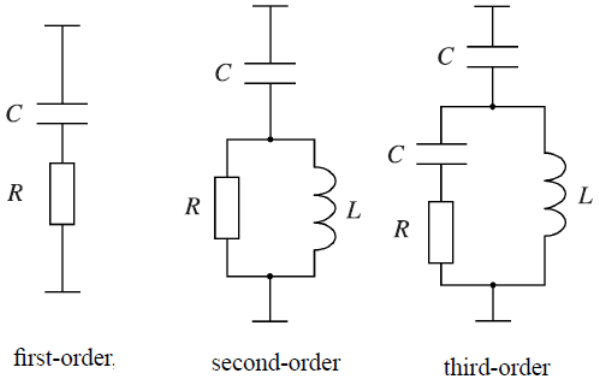


Figure 2-4: Typical Passive High-pass Filters

The major disadvantage of the passive filters is that they are designed for a specific load. This means their filtering efficiency is strongly affected as soon as the load power varies since the system resonance varies with the impedance. Moreover, components like capacitors are negatively affected over the time. This causes a shift of the filter resonance inducing a decrease of the filter performance over the time. However, they are still widely produced and used especially for specific well-designed usage as presented in the appendices in paragraph 8.1

2.2 Active Harmonic Filters

Unlike the passive harmonics filters, active harmonic filters also called active power filters (APFs) is a relatively recent technology but has quickly become mature [35] [36]. Their basic operating principles have drawn major interest in the 1970s as the harmonic pollution in the power systems was of more and more concern. Their fast emergence has been boosted by the development of powerful and efficient power electronic devices such as IGBTs and MOSFETs that are controllable fast switching devices. This has been complemented by the development of Digital Signal Processor (DSPs) and Field Programmable Gate Arrays (FPGAs) as well as analogue to digital converters (ADCs). The technology of the APF is now mature as it provides more usage than just the harmonics mitigation. The APFs can actually be considered as power conditioner as they can additionally serve as reactive power compensators, unbalance current correctors in three-phase systems, supply voltage magnitude regulators including flicker mitigation. That is the reason why the modern APFs are widely preferred compared to the traditional passive filters. They provide a better overall performance as they are smaller and more flexible (compared to passive filters) concerning the number, the magnitude and the frequency of harmonics that they can eliminate.

The APFs are basically classified based on their designed voltage system: single-phase or three-phase voltage system. Three-wire and four-wire configurations are considered subcategories

of the three-phase category. A further classification can be done by distinguishing the type of the inverter used which can be either current fed (current source inverter – CSI) or voltage fed (voltage source inverter – VSI). The APF topology, defining how the APF is connected to the grid, is another differentiation parameter as the controlled inverter can be a series or shunt active filter or a combination of both. The appendices in paragraph 8.2 provide an overview of actual active power filters currently available on the market including their main characteristics and features.

2.2.1 Classification Based on the Operating Voltage System

2.2.1.1 Single-phase APF

Nowadays, most of the domestic appliances are typical single-phase nonlinear loads that everyone uses at least once per day. These appliances are in general electronic devices, where the AC supply voltage is transformed into another form (mostly DC voltage) or the current draw is imposed by switching elements. The most popular are radio and TV's, computers, printers, batteries chargers, light dimmers, energy efficient lamps and video game consoles. Multiple single-phase APFs configurations and control techniques are presented in [35] [37] [38] [39] [40]. The typical circuit configuration of a single-phase APF is shown in Figure 2-5 [41]. It can be considered as a standard H-bridge inverter, whose load is the voltage source to clean and the power source is the capacitor. The DC capacitor represents the energy supply of the APF and therefore is fed by another voltage source such as photovoltaic panels, battery bank, or wind or hydraulic turbine or even a DC-AC voltage converter.

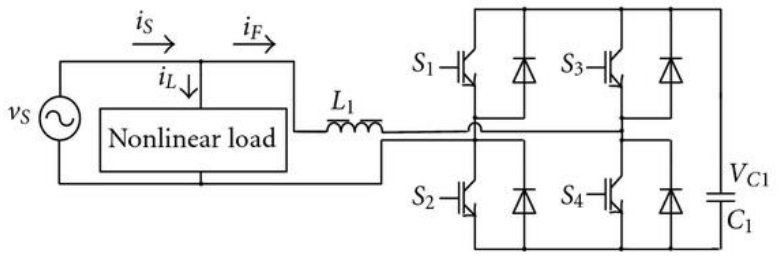


Figure 2-5: Configuration of a Single-phase APF

2.2.1.2 Three-phase APF

Three-phase APFs are designed for three-phase nonlinear loads such as adjustable speed drives. Since the biggest amount of electrical energy is produced, transmitted, distributed and consumed as three-phase voltages, single-phase APFs are less popular than three-phase APFs. Many publications reporting on three-phase APFs exist already since 1976 [36] [42] [43] [44] [45]. They present various detection methods still in use today such as the synchronous frame theory and notch filters (band-stop filters) [46] [47]. Three-phase voltage systems come with a major additional issue, which is the unbalance. Therefore, many developed three-phase APFs incorporate load balancing and neutral line current cancellation for three-phase four wire configurations [48] [49]. The publication in [50] gives a detailed analysis and comparison of typical 4-wire APFs. The first configuration (Figure 2-6 [51] [52]), known as the capacitor mid-point configuration is used only for small current values since all the neutral current, that can be considerably high, flows through the capacitors. The second configuration (Figure 2-7 [53]) is implemented in order to stabilize the neutral point of the APF through the 4th branch. The third and most common configuration (Figure 2-8 [54]) improves the reliability of the APF

system as the voltage of the solid-state device is properly matched. It is comparable to three distinct single-phase H-bridge inverter having the neutral line as common point. Despite doubling the number of switching elements, this configuration brings a higher flexibility as each phase voltage can be controlled independently of the others.

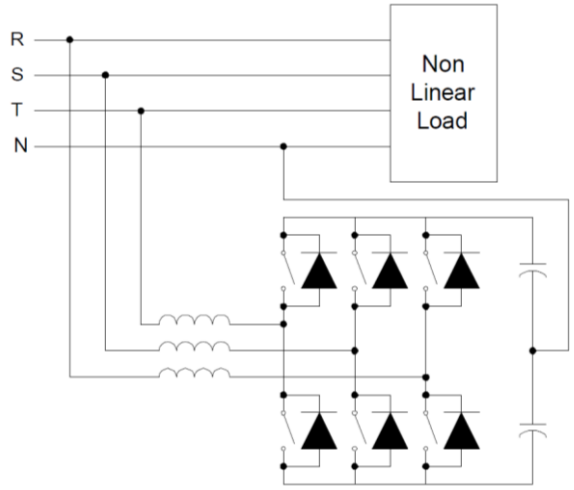


Figure 2-6: Configuration of Capacitor Midpoint Four-wire APF

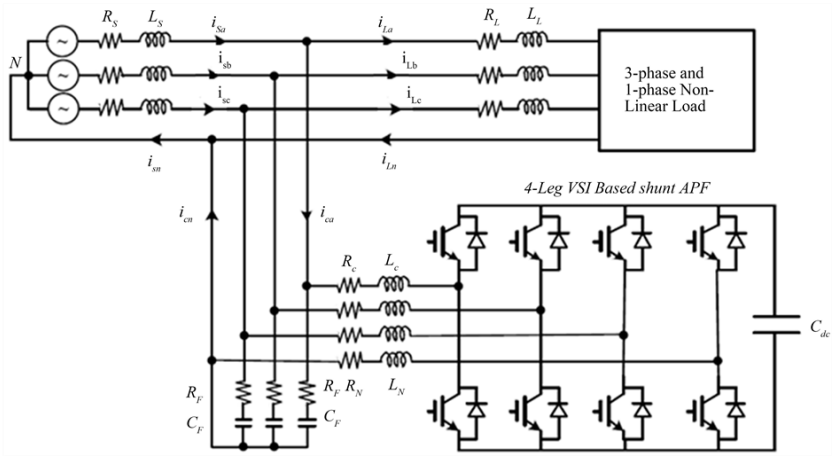


Figure 2-7: Configuration of a Three-phase four-wire APF (hybrid)

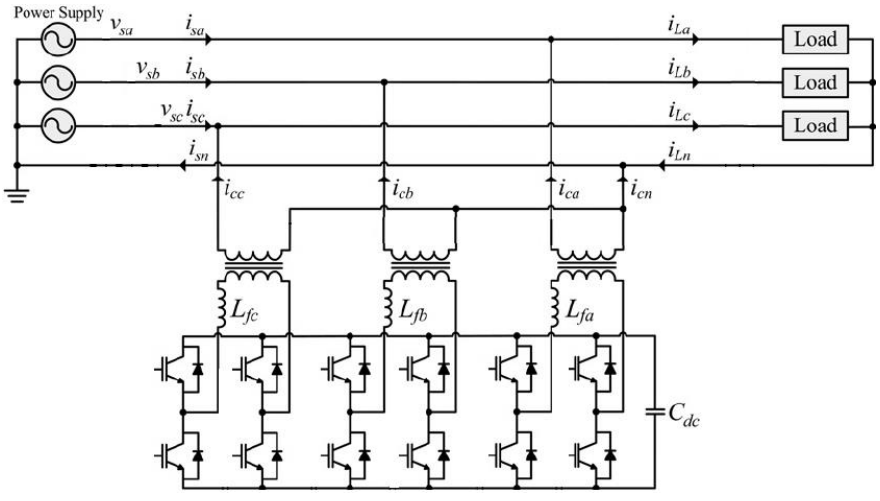


Figure 2-8: Configuration of a Three-bridge four-wire APF

2.2.2 Classification Based on the Type of Inverter

2.2.2.1 Current Source Inverter

The CSIs can be considered as current harmonics sources that are controlled in order to meet the current harmonics requirement of a harmonic-producing load. Their structure is depicted in Figure 2-9 [31]. It requires an AC capacitor that is connected in parallel. A CSI uses an inductive energy storage system, which is an inductor. The inverter commutating devices can be IGBTs with reverse blocking diodes or GTOs (most of the time). The GTOs-based CSIs appear to be more reliable, but they are constrained to lower switching frequencies and present considerably high switching losses [55].

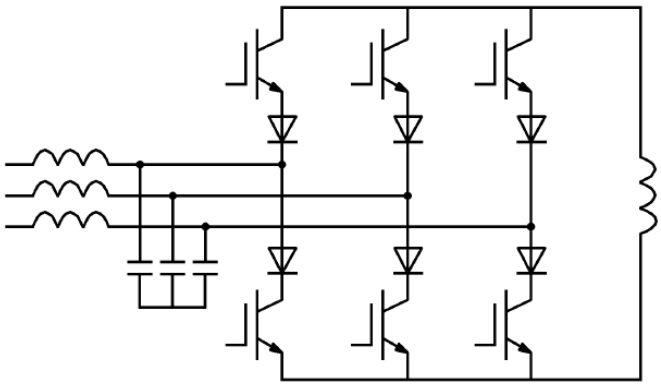


Figure 2-9: Typical Circuit of a Current Source Inverter

2.2.2.2 Voltage Source Inverter

Very similar to the CSI in the circuit structure, the VSIs use capacitors as energy storage elements (Figure 2-10 [31]). They generate PWM voltages including the frequencies of the harmonics to be mitigated. Here, the most common switching devices used are IGBTs that are more efficient than GTOs used for CSIs. Despite the large DC capacitor required, VSIs are most popular than CSIs because they are smaller (lighter), more efficient (cheaper) and easily expandable. VSI-based APFs can also be easily integrated into the main grid system as it can directly use the grid power to feed its DC capacitor link in order to eliminate the harmonic disturbances on the same grid.

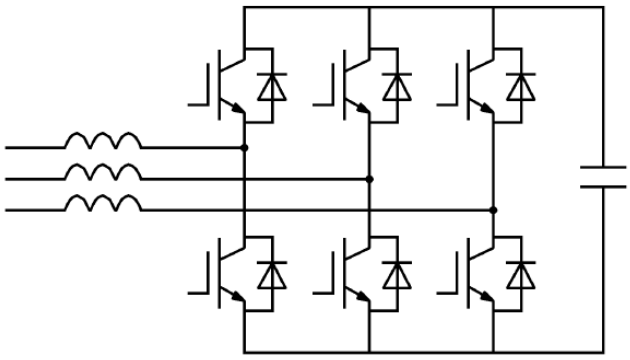


Figure 2-10: Typical Circuit of a Voltage Source Inverter

2.2.3 Classification Based on the Topology

2.2.3.1 Shunt Active Power Filters

The way the shunt APFs are connected with another voltage source is depicted in Figure 2-11 [52]. It is designed to compensate the current harmonics by generating and injecting opposite current harmonics into the system.

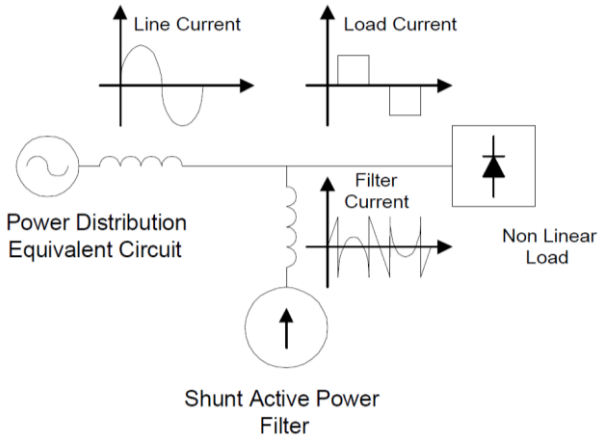


Figure 2-11: Basic Single-phase or Three-phase Shunt APF Connection to the Power Grid

This makes the power distribution system to supply an almost pure sine current and therefore sees the nonlinear load and the APF as a perfect linear load (resistor). The shunt APFs are also widely used as power factor controller (reactive power compensation – similar to STATCOM) and currents balancing for three-phase voltage system [31].

2.2.3.2 Series Active Power Filters

The basic block configuration of series APFs is depicted in Figure 2-12 [31]. They are basically designed to mitigate voltage harmonics. They are connected in series with the utility grid through a transformer before the load. The series APF acts as a zero impedance for the fundamental frequency but a very high impedance for the harmonic voltages. This is done by generating voltages of the same frequency as the harmonics to eliminate. Voltage unbalance in three-phase systems can also be corrected using series APFs [56].

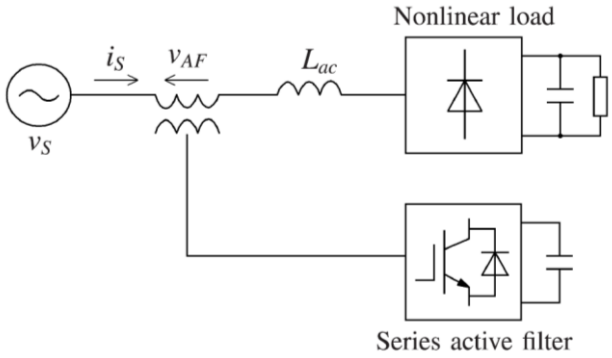


Figure 2-12: Basic Single-phase or Three-phase Series APF Connection to the Power Grid

2.2.3.3 Unified Power Quality Conditioners

UPQCs (topology depicted in Figure 2-13 [57]) combine the series and the shunt APF with a shared DC link source. It allows the simultaneous mitigation of numerous voltage and current disturbances. The concerned disturbances go beyond the harmonics and power factor (which

can be controlled by single series or shunt APF) as voltage sags or swells, over-and undervoltages can also be mitigated. In three-phase systems, voltages and current unbalance as well as neutral currents in three-phase four-wire configuration (inherited ability from the single series and shunt APF) are compensated. The main disadvantage of the UPQC is their high cost especially due to the number of solid-state devices in use and the complex control to implement [56]. They are mainly used by power voltage suppliers, industries requiring fully controlled voltage quality such as electronic devices manufactures and power sensitive building like hospitals.

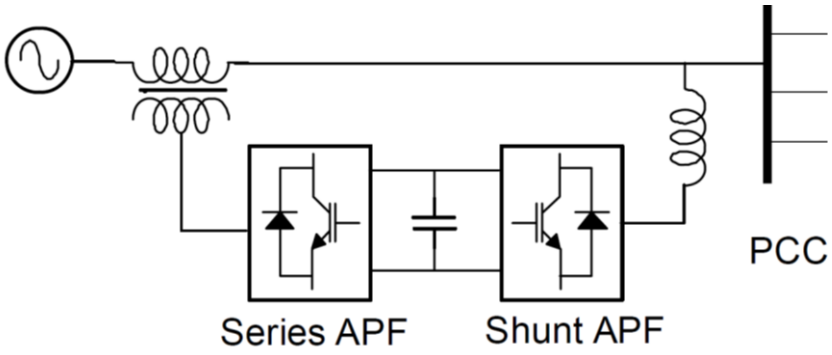


Figure 2-13: Basic Single-phase or Three-phase UPQC Connection to the Power Grid

2.2.3.4 Hybrid Active Power Filters

The hybrid filters represent the most popular topology of the APFs systems. It is the combination of a pure active filter and a pure passive filter. There are several possible hybrid configurations presented in [58] but in general, the goal is to achieve the mitigation of the lower order harmonics with the passive filter, while the active filter part eliminates the high order harmonics as shown in Figure 2-14 and Figure 2-15 [31]. The main advantage of hybrid APF is the filter optimized cost since it allows the reduction of the active filter rating (which is most expensive than the passive filter part) [59].

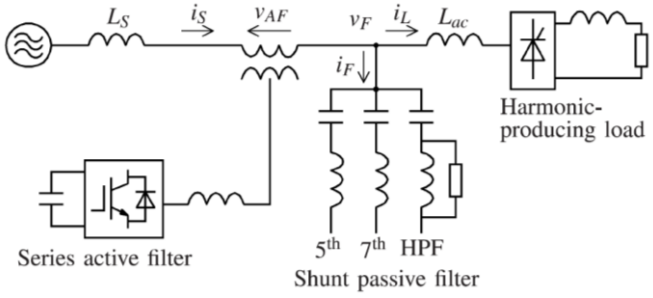


Figure 2-14: Hybrid APF with Series Active Filter and Shunt Passive Filter

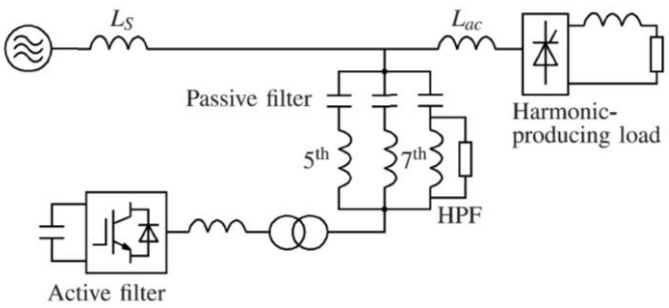


Figure 2-15: Shunt Hybrid APF Block

Transformerless and low-voltage hybrid active filters are presented in [31] as shown in Figure 2-16. They are designed to be connected directly to the low-voltage distribution grid without any transformer. This design can be divided into two main parts, which is the capacitors and the active filter that includes the inductors and the PWM controlled VSI. This configuration allows the DC link voltage feeding the inverter to be considerably lower compared to the standard pure active filter design (same as Figure 2-16 except the capacitor C_F) as the comparative study in [31] shows. However, this requires large capacitors that make the system bulky and expensive.

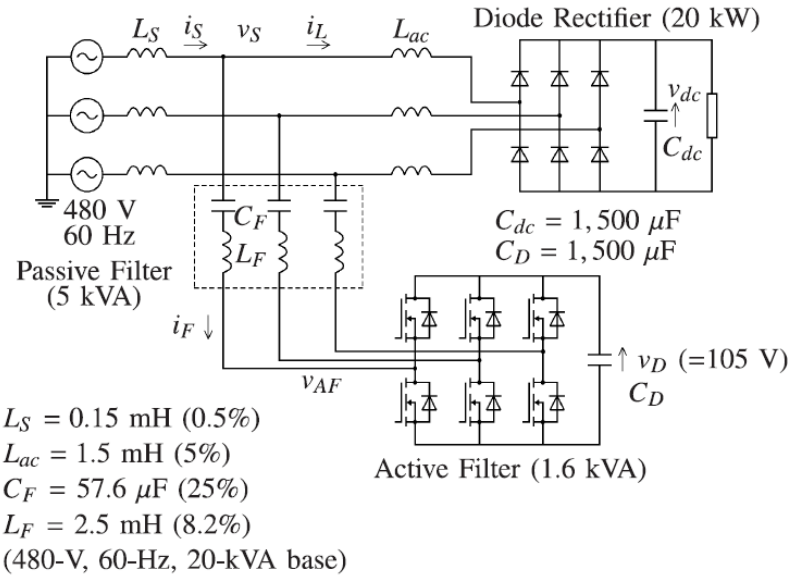


Figure 2-16: Configuration of a Transformerless Low-voltage Hybrid Active Filter

2.3 Conclusion

The evolution of the harmonics filtering in the power grid is strictly bound to the increasing complexity of the used electric appliances. The harmonics became a major issue for the power supply with the emergence of electronics or electronically controlled equipment. Passive power filters are the oldest and simplest method developed and are still used to eliminate the harmonics, especially in transmission and distribution grids. The development of active power filters has been boosted by the development of more efficient power electronic components as well as sensors, FPGAs, fast actuators and switching devices. They are basically electronic devices used to counter the effects of other electronic devices on the grid voltage. Very flexible concerning the range of harmonics filtering ability, the active power filters offer several additional capabilities, so that they are now considered as power conditioners. Inheriting the full power of electronics, active power filters can simultaneously compensate the harmonics, regulate the voltage magnitude at the point of common coupling by mitigating voltage swells or dips, over- as well as under-voltages. Furthermore, they can serve as power factor controller by regulating the reactive power flowing through the grid. All these features make the active filters relatively expensive. However, the best cost effective filters have been proved to be hybrid active power filters that combine passive and active filters.

3 Harmonics Identification Methods for Active Power Filters

The previous chapter has shown how harmonics can be mitigated by using active filters. However, none of these would work properly without a good, fast and accurate detection method. Detection is the key! This chapter presents an overview of different harmonics detection methods.

3.1 The Frequency Domain Methods

3.1.1 The Discrete Fourier Transform

The Fourier transform is based on the fact that any periodical signal can be decomposed into a sum of different sinusoidal functions (represented in the complex range) each having a given amplitude, frequency and phase shift. The first sinusoidal function is the fundamental signal and the rest are its harmonics, this means that their frequencies are integer multiples of that of the fundamental. The Discrete Fourier Transform (DFT) is a tool that helps to transform discrete periodical signals (like distorted alternative voltages or currents) into a corresponding mathematical expression that gives information on both the amplitude and the phase shift of any harmonic signal present. This method is defined by:

$$\bar{X}_h = \sum_{n=0}^{N-1} x(n) \cdot \cos\left(\frac{2\pi \cdot h \cdot n}{N}\right) - j \cdot \sum_{n=0}^{N-1} x(n) \cdot \sin\left(\frac{2\pi \cdot h \cdot n}{N}\right) \qquad (3\text{-}1)$$

Where $\bar{X}_h$is the complex Fourier vector of the harmonic h contained in the input signal. N represents the number of samples corresponding to one fundamental period, $x(n)$ is the input signal at the point n.

Composed of a real term and an imaginary term,

$$X_{hr} = \sum_{n=0}^{N-1} x(n) \cdot \cos\left(\frac{2\pi \cdot h \cdot n}{N}\right);\ X_{hi} = -\sum_{n=0}^{N-1} x(n) \cdot \sin\left(\frac{2\pi \cdot h \cdot n}{N}\right) \qquad (3\text{-}2)$$

The amplitude $|\bar{X}_h|$ and the phase φ_h of the harmonics can be obtained by

$$|\bar{X}_h| = \sqrt{(X_{hr})^2 + (X_{hi})^2};\ \varphi_h = \arctan\left(\frac{X_{hi}}{X_{hr}}\right) \qquad (3\text{-}3)$$

The principal drawback of this method is the huge number of additions and multiplications needed to deliver valid values. Moreover, the finally valid output occurs only, at the most, once every fundamental period. This makes this method adequate only for quite steady systems experiencing very slow changes or disturbances.

3.1.2 The Fast Fourier Transform - FFT

The FFT was developed in order to reduce the number of calculation needed for the DFT. It is very similar to the DFT but uses the decimation technic that is based on the decomposition of an N point DFT into a 2 points transform of N/2. This can be applied to any N sample points signal as long as N is a number integer power of 2.

3.1.3 The Recursive Discrete Fourier Transform – RDFT

This method has exactly the same working principle as the DFT except that the calculations are permanently done within one sliding window of samples. For each new input sample, the oldest sample is eliminated and the calculations are realised with the new set of samples. The

only difference between two consecutive sets of samples is the first and last sample in each set. Since a result has already been calculated for the previous set of samples, a recursive expression (3-4) is used to avoid the same series of calculations for the new set of data.

$$\bar{X}_h = \frac{1}{N} \cdot \sum_{i=0}^{N-1} x(i) \cdot W^{-hi}, with\ W = e^{\left(j \cdot \frac{2\pi}{N}\right)}$$
$$X_h(k) = \frac{1}{N}\big(x(k) - x(k-N)\big) + W^h \cdot X_h(k-1) \qquad (3\text{-}4)$$

This recursive expression can be written in the form of a transfer function as.

$$H_h(z) = \frac{X_h(z)}{x_h(z)} = \frac{1}{N} \cdot \frac{1 - z^{-N}}{1 - W^h z^{-1}} \qquad (3\text{-}5)$$

This transfer function corresponds to a finite impulse response (FIR) filter. This is very convenient for a selective harmonic detection from the input signal.

3.2 The Time domain methods

3.2.1 The Synchronous Reference Frame (SRF)

Designed for 3-phase power systems, this method represents the main core of many other derived detection algorithms. The working principle of this method is based on the transformation from a 3-axis stationary frame to a 2-axis orthogonal rotating frame. The harmonic detection process can be divided into 3 steps.

- Transformation of the 3-axis system values (measured 3-phase voltages or currents) into the fix orthogonal αβ-frame through the Clarke transformation
- The values obtained in the αβ-frame are then transformed into the rotating dq-frame through the Park transformation. The angular velocity of the dq-frame is equal to the angular velocity of the 3-phases voltages system. This step requires the actual phase angle of the voltages. Therefore, a phase detector, which is mostly a PLL (Phase-Locked Loop), is needed. The resulting values $V_d$and $V_q$consist of two terms each, the fundamental values, which represent DC components $(\bar{V}_d, \bar{V}_q)$ and the harmonic components $(\tilde{V}_d, \tilde{V}_q)$ that include all harmonics, is the AC component.
- A high-pass filter (HPF) is then used to extract the harmonic components and they can now be used to generate the compensation signal with the help of the inverse Park and the inverse Clark transformation matrices.

The SFR detection method can be well summarized as a block diagram as shown in Figure 3-1.

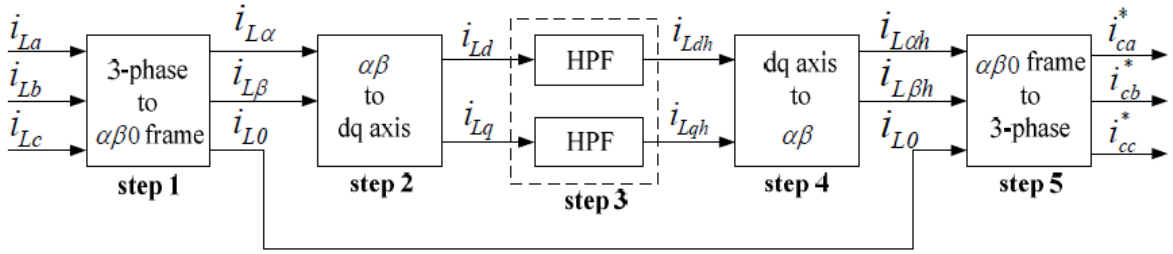


Figure 3-1: Method's Summary of the SFR Harmonics Compensating Method

One method derived from this SRF method is the Selective Harmonic Synchronous Reference Frame SHSRF (Figure 3-2). The particularity of the SHSRF is that the different harmonic signals

are detected separately. This means that one can choose which harmonic to consider and which one not. The difference of the SHSRF compared to the SFR is that the fundamental angular velocity is now replaced by that of each selected harmonic to be compensated. In the dq-frame, the obtained values also consist of 2 terms but only the DC components correspond to the chosen harmonics values. The extraction of these DC components is done using a low-pass filter (LPF).

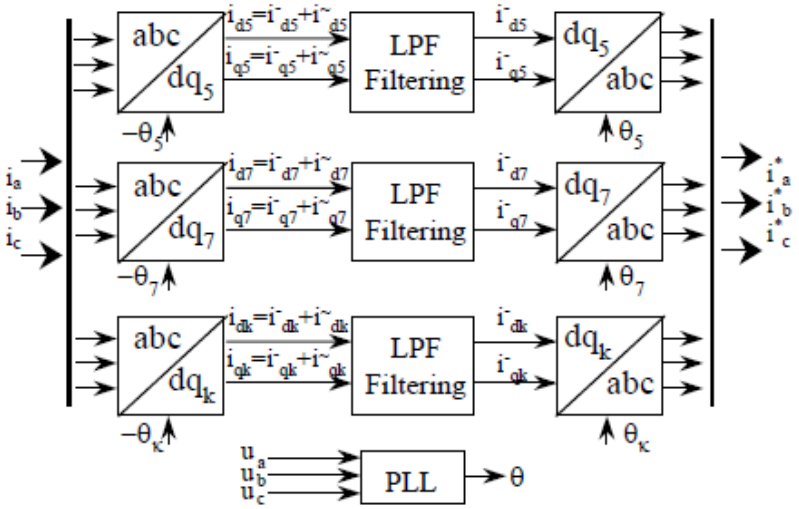


Figure 3-2: Method's Summary of the SHSFR Harmonics Compensating Method

The weak point of these methods relies on the fact that they need the actual phase angle for their computations. This is delivered by a PLL that requires a precise implementation and which is unfortunately negatively influenced by any voltage unbalance. Another important issue is the implementation of the numerical LPFs and the HPFs. They generate phase shifts that should be taken into consideration in the generation of the compensation values.

3.2.2 Instantaneous Reactive Power Theory (IRPT)

This method determines the harmonic distortion using the instantaneous power calculation of the 3-phase system. The active and reactive powers are the result of the product of the voltage and current values in the αβ-frame as in (3-6).

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \qquad (3\text{-}6)$$

As in the SFR method, the P and Q value consist of DC and AC components. Once the DC components are removed by an HPF, the remaining AC components represent all the harmonic components creating the current distortion. These values computed back into the 3-phase abc frame, constitute the current compensation values.

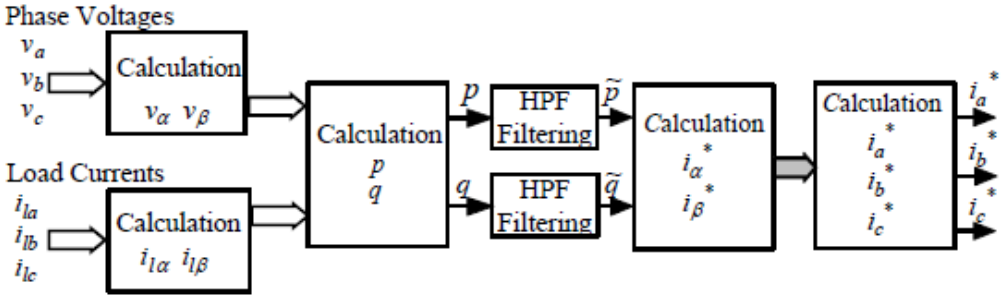


Figure 3-3: Method's Summary of the IRPT Method

Also here, the use of a numerical HPF has an influence on the dynamic and the accuracy of the detection system.

Another method very similar to the IRPT called the Synchronous Detection Method SDM is based on the direct calculation of the instantaneous real power. This method can be distributed in the following steps and is well depicted as a block diagram in Figure 3-4.

- Under the assumption that the power system is balanced, the total apparent power S is calculated as follows.

$$S = v_a \cdot i_{la} + v_b \cdot i_{lb} + v_c \cdot i_{lc} \tag{3-7}$$

- The average power value S_{dc}, which corresponds to the DC component of the apparent power, is extracted using a LPF
- The three phases reactive power can be calculated by:

$$\begin{bmatrix} Q_a \\ Q_b \\ Q_c \end{bmatrix} = \frac{S_{dc}}{\hat{v}_a + \hat{v}_b + \hat{v}_c} \cdot \begin{bmatrix} \hat{v}_a \\ \hat{v}_b \\ \hat{v}_c \end{bmatrix} \tag{3-8}$$

  Where $\hat{v}_a, \hat{v}_b \; and \; \hat{v}_c$ are the amplitudes of the line voltages a, b and c respectively.
- The source currents are then calculated as follows using the line voltage values and the calculated reactive power. The compensation currents are finally calculated by subtracting the computed source currents from the measured load currents.

$$\begin{cases} i_{sa} = \dfrac{2v_a \cdot Q_a}{v_a^2} \\ i_{sb} = \dfrac{2v_b \cdot Q_b}{v_b^2} \\ i_{sc} = \dfrac{2v_c \cdot Q_c}{v_c^2} \end{cases} \rightarrow \begin{cases} i_{ca} = i_{la} - i_{sa} \\ i_{cb} = i_{lb} - i_{sb} \\ i_{cc} = i_{lc} - i_{sc} \end{cases} \tag{3-9}$$

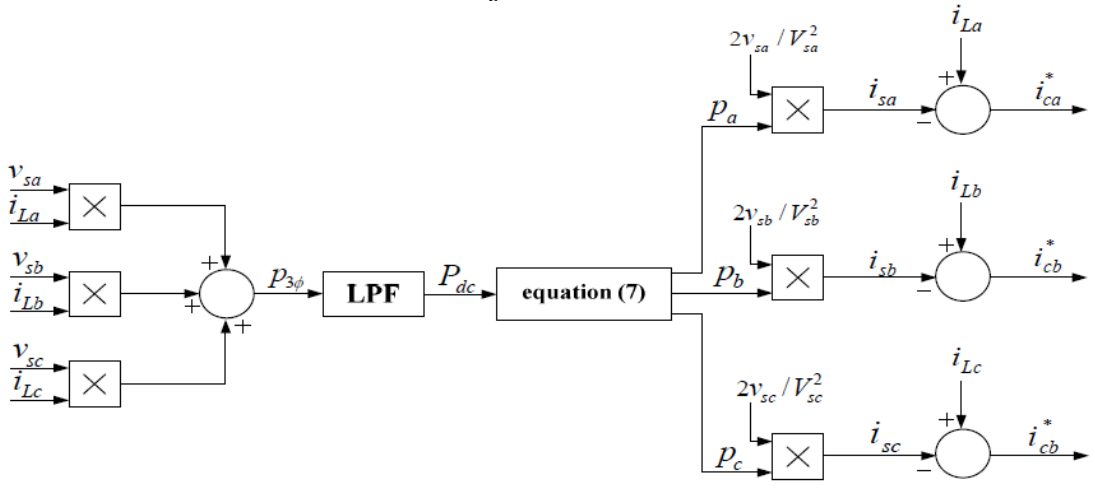


Figure 3-4: Method's Summary of the Synchronous Detection Method

3.2.3 The Synchronous Reference Frame with the Fourier transform DQF

This algorithm puts together the advantages of the SRF methods and the Sliding Window Fourier Analysis (SWFA). The SRF method is used to compute the current dq-components and the SWFA to separate the fundamental currents from the harmonic currents. The whole process, depicted in Figure 3-5, can be described in the following steps

From the SRF method,

- The distorted currents of the three phases are transformed to the stationary αβ-frame.
- Then the current values in the αβ-frame are transformed in the synchronously rotating dq-frame

Using the SWFA method,

- The components of the harmonic currents are separated from those of the fundamental current using the SWFA method. The SWFA is based on the Euler-Fourier formula given as a sum of a DC and an AC component.

$$i_l(kt) = \frac{A_0}{2} + \sum_{h=1}^{\infty} [A_h \cos(h\omega kT) + B_h \sin(h\omega kT)] \quad (3\text{-}10)$$

A_0, A_h and B_h are the Fourier series coefficients, ω is the angular velocity of the fundamental signal, h is the harmonic order, T is the sampling time period in second and k is the time index. Since it is faster to calculate only one coefficient, the SWFA helps computing only the DC component. Therefore, only the A_0 coefficient is to be determined and this is done by setting h to zero in the following formula.

$$A_h = \frac{2}{N} + \sum_{n=N_0}^{N_0+N-1} i_l(nT) \cos(nh\omega T) \quad (3\text{-}11)$$

The components of the fundamental currents can be obtained by

$$\begin{cases} \bar{\imath}_{ld}(kT) = \dfrac{A_{0d}}{2} \\ \bar{\imath}_{lq}(kT) = \dfrac{A_{0q}}{2} \end{cases} with \begin{cases} A_{0d} = \dfrac{2}{N} + \sum_{n=N_0}^{N_0+N-1} i_{ld}(nT) \\ A_{0q} = \dfrac{2}{N} + \sum_{n=N_0}^{N_0+N-1} i_{lq}(nT) \end{cases} \quad (3\text{-}12)$$

N_0 is the first sample and N is the total number of samples points in one cycle. Integrating the recursion of the sliding window, the updated values are given by

$$\begin{bmatrix} A_{od}^{(new)} \\ A_{oq}^{(new)} \end{bmatrix} = \begin{bmatrix} A_{od}^{(old)} \\ A_{oq}^{(old)} \end{bmatrix} - \frac{2}{N} \begin{bmatrix} i_{ld}(N_0 - 1)T \\ i_{lq}(N_0 - 1)T \end{bmatrix} + \frac{2}{N} \begin{bmatrix} i_{ld}(N_0 + N)T \\ i_{lq}(N_0 + N)T \end{bmatrix} \quad (3\text{-}13)$$

- Once the components of the fundamental signal are found, the harmonics components are obtained by subtracting the values of the fundamental from the measured current values

$$\begin{cases} \tilde{\imath}_{ld} = i_{ld} - \bar{\imath}_{ld} \\ \tilde{\imath}_{lq} = i_{lq} - \bar{\imath}_{lq} \end{cases} \quad (3\text{-}14)$$

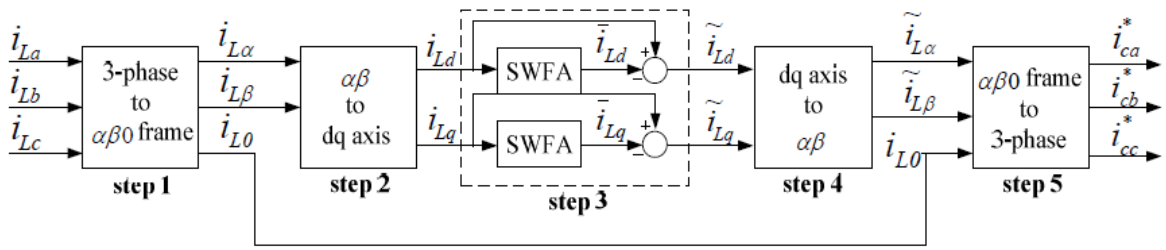


Figure 3-5: Method's Summary of the DQF Method

3.2.4 The Generalized Integrator

The generalized integrator approach is depicted in Figure 3-6. It behaves as a number of parallel band-pass filters that extract only the harmonic wave corresponding to the filter characteristic. The most critical issue is the optimisation of the integrator constant. Choosing a small value gives a very good filtering efficiency but in contrast, results in a slow dynamic response. This method is mostly used in single-phase voltage system for generating the β-component (90° phase-shifted) of the input signal. These values are then the input for dq-based PLLs. The major advantage of such an approach is that the output values are well filtered and therefore do not influence the other harmonics signals. The Generalized integrator can also be extended so that it delivers additional information such as the input voltage magnitude and phase-angle as well as the frequency [60].

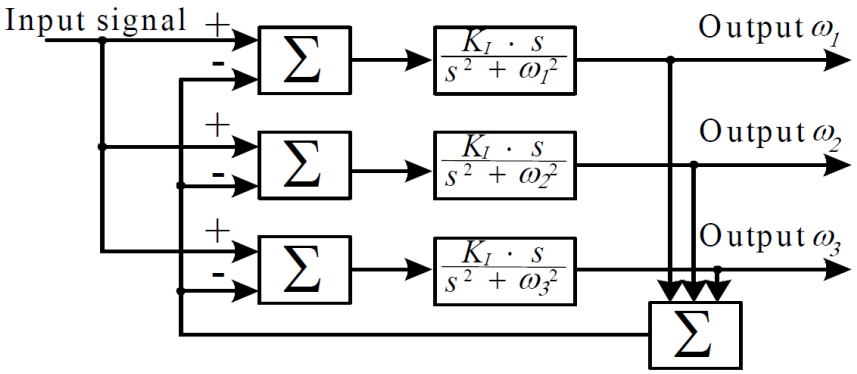


Figure 3-6: Method's Summary of the Generalized Integrator Method

3.3 Conclusion

There are many different harmonic detection algorithms. Each of them has its strengths but also its disadvantages. The right and optimal detection method depends mostly on the application type. Real-time applications such as signal generation and control or power filtering prioritize fast detection methods such as the IRPT or SRF. Choosing the best appropriate algorithm then relies on the microcontroller computational power that fixes the total number of operations and the precision of the calculation. Slow changing systems and also non-critical operations like post-processing can work properly with algorithms having a lower dynamic. However, the trend nowadays is toward the fast and dynamic methods thanks to the technological progress in electronics (faster and more accurate sensors, improved power electronics elements) and microcontrollers, which are getting faster and faster.

4 Phase-Locked Loop Based Sinusoidal Signal Identification

In addition to the magnitude, a very important value for almost all the time domain harmonic detection methods, as well as the compensation methods, is the phase angle of the signal. Any other computed value like the compensatory voltages and/or currents can quickly become useless if the timing is not respected. Respecting the timing for alternating signals means knowing very well the phase angle of the signal. The Phase-Locked Loop (PLL) is a tool that helps to detect the instantaneous phase angle of the input voltages or currents.

Originally, the concept of the PLL was used essentially in telecommunication for the synchronous reception of radio signals. The first publications on that concept appeared in 1923 and 1932 and were made by Appleton and Bellescize respectively [61] [62]. Later on, the use of the PLL techniques spread widely in many other fields such as the induction heating power supply [63], the motor control systems [64], the contactless power supplies [65] and the communication systems [66] [67] [68]. Nowadays, their usability has been strengthened by the synchronization need of many different power systems. There exist many different PLLs algorithms that can be primarily separated into two large groups: the 3-phases PLLs and the single-phase PLLs. Another good differentiation criterion is the number of possible signal information delivered by the PLL. So we can also distinguish the PLL delivering only the angular velocity (the frequency) and the phase angle of the signal, while others also calculate the signal amplitude in addition to its phase angle and angular velocity. This chapter presents first briefly some PLLs algorithms and in a second step, a focus is made on the algorithms based on SRF transformation since they deliver valuable DC values that can be used for a control purpose (like for a harmonic amplitude controller like the APF).

4.1 The Three-Phase PLLs

4.1.1 The Synchronous Reference Frame PLL dqPLL

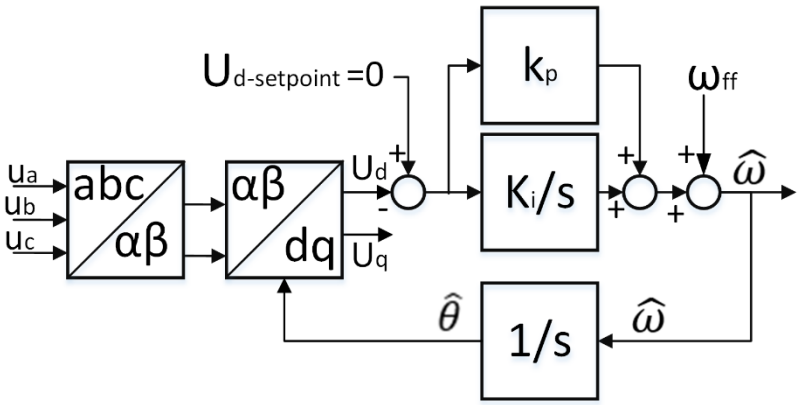


Figure 4-1: Block diagram of the dqPLL

The working principle of the dqPLL, depicted in Figure 4-1 [69] is based on regulating the voltage direct component U_d in the rotating dq-frame to zero. The α- and β-voltage components obtained from the Clark Transform are transformed into the d-q rotating frame and the direct component is regulated through a PI controller to zero, while the quadrature component U_q converges to the signal magnitude and the controller output value is the estimated angular velocity of the d-q rotating frame. U_d is calculated using the estimated

phase angle that is the integrated value of the estimated angular velocity. In a balanced and harmonic free system, U_d and U_q are expressed as:

$$\begin{bmatrix} U_d \\ U_q \end{bmatrix} = \begin{bmatrix} \sin\hat{\theta} & -\cos\hat{\theta} \\ \cos\hat{\theta} & \sin\hat{\theta} \end{bmatrix} \cdot \begin{bmatrix} U_\alpha \\ U_\beta \end{bmatrix} \quad (4\text{-}1)$$

$$Where \begin{cases} U_\alpha = \hat{U}\cos\theta \\ U_\beta = \hat{U}\sin\theta \end{cases} and\ \hat{U}\ is\ the\ input\ signal\ magnitude$$

Then

$$\begin{cases} U_d = U\cos\theta\sin\hat{\theta} - U\sin\theta\cos\hat{\theta} \\ U_q = U\cos\theta\cos\hat{\theta} + U\sin\theta\sin\hat{\theta} \end{cases} \rightarrow \begin{cases} U_d = -U\,sin(\theta - \hat{\theta}) \\ U_q = U\cos(\theta - \hat{\theta}) \end{cases} \quad (4\text{-}2)$$

The equations (4-1) and (4-2) confirm well that when the estimated phase angle $\hat{\theta}$ is nearing the real phase angle θ, U_d is approximately zero, while U_q tends to the input voltage magnitude. The complete dynamic of the detection system depends on the controller gains k_p and k_i. These coefficients play another important role when it comes to harmonics rejection capabilities of the system. If the input voltages are distorted due to harmonics, the dqPLL still works but the output values are oscillating. The impact of the harmonics on the output values can be reduced by adjusting the controller parameters. If the bandwidth of the PI controller is reduced, the system is less sensitive to the harmonics distortion but less dynamic too. A good compromise must be found between the precision and the response speed. In case of voltage unbalance, there is however no detection improvement realized through the bandwidth reduction [70] [71].

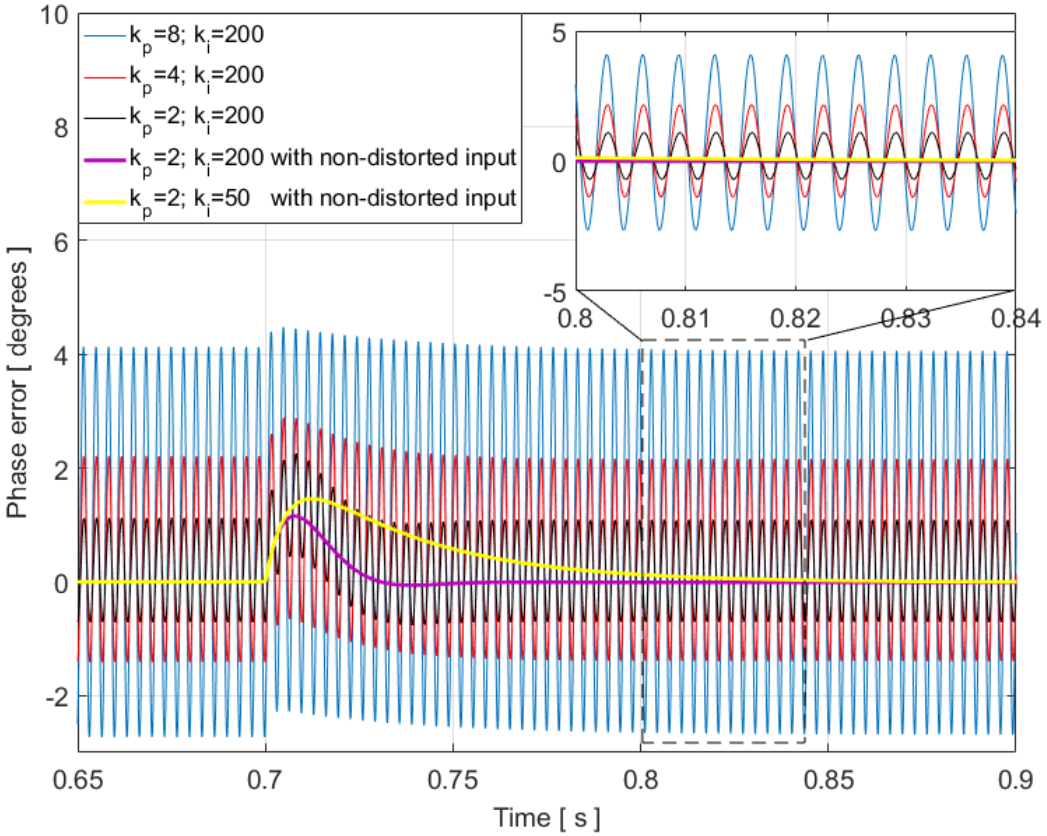


Figure 4-2: dqPLL's Phase Error Dynamic and Harmonics Rejection

The Figure 4-2 depicts the impact of different values of the PI-controllers coefficients on the estimated phase error computed by the dqPLL. These are obtained for a three-phase sinusoidal input signal with a 50Hz frequency and a magnitude of 100V. The 5th and 7th harmonics with magnitudes of 30V and 15V respectively are injected into the input signal. At the time 0.7 sec, the frequency of the input signal is increased by 2%. It can be noticed that the parameter k_i affects mostly the response time. The greater its value the faster the system. The maximum value of the phase error is slightly lower, when k_i is greater. The harmonics rejection ability, characterised by the level of oscillation of the estimated phase-angle error delivered by the system, is determined by k_p. With the same k_i, the peak value of the oscillating phase error is proportional to the k_p parameter as it is reduced from 4 to 1 degree when the k_p decreases from 8 to 2.

The frequency spectrum of the oscillating phase error depends on the harmonics contents of the input signal. The following theoretical analysis depicted in Figure 4-3 shows, for a three-phase system, that harmonics contained in the computed phase error are always even multiples of the fundamental frequency of the input signal. They can be described as

$$\begin{cases} f_{h_{\Delta\theta}} = f \times (n+1) \\ f_{h_{\Delta\theta}} = f \times (m-1) \end{cases} \quad (4\text{-}3)$$

Where n is the order of the harmonic with negative sequence, m that of the positive sequence and f the fundamental frequency. This means that two consecutive harmonics of the same pair (5th - 7th, 11th - 13th, 17th - 19th etc.) both generate the same harmonic in the PLL calculations. The results shown in Figure 4-3 are the input and the delivered signal of a dqPLL where the fundamental frequency of the input voltage signal has a magnitude of 100V. The distorting 5th, 7th and 11th harmonics respectively have the magnitude of 30V, 20V and 10V. This is clearly shown in the frequency spectrum of the input signal. The 5th and 7th harmonics have a combined effect on the direct component calculation as it results in a 10V and 300 Hz signal. The 11th harmonic causes the appearance of the 12th harmonic (600 Hz) in the U_d value. These frequencies are the ones distorting the final phase-angle error value delivered by the PLL.

A second analysis has been realized (Figure 4-4) with a different harmonic distortion. In this case, the 5th harmonic with a magnitude of 30V is still present combined with the 13th and the 17th harmonic with the magnitude of 20V and 10V respectively. Since there is no harmonic pair, the frequency spectra of U_d as well as $\Delta\theta$ depict the three distinct 6th, 12th and 18th harmonics. It is very difficult to extract valuable information concerning the harmonic spectrum of the input signal from the calculated U_d and $\Delta\theta$ values, because one appearing harmonic in the PLL calculations results from the combination (in frequency and magnitude) of one harmonics pair. For example, the 6th harmonic (300 Hz) with a magnitude of 10V in the U_d frequency spectrum in Figure 4-3 is induced at the same time by the 5th and 7th harmonics contained in the input signal whereas, the 6th harmonic in Figure 4-4 with a magnitude of 30V comes from only the 5th harmonics. The 5th and 7th harmonics, similar to others harmonics pairs, have counteracting effects on the magnitude of the resulting 6th harmonic. This intrinsic property could be used to improve the harmonics rejection of the whole PLL.

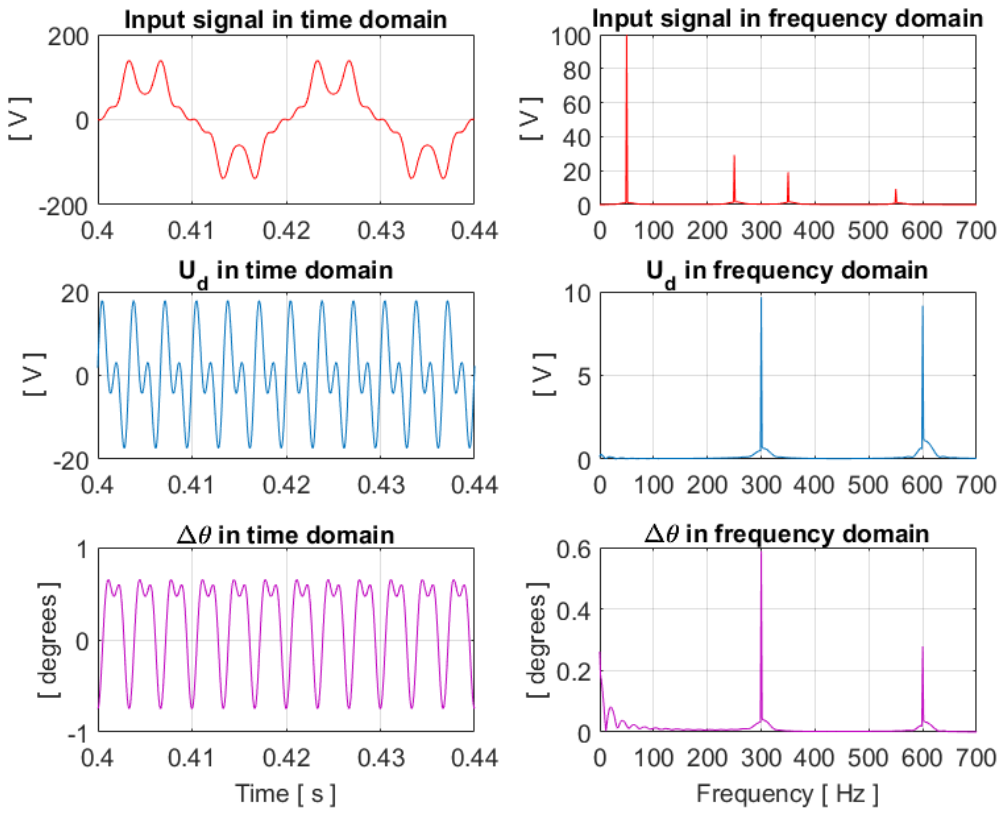


Figure 4-3: Time and Frequency Domain of the PLL Input Signal, U_d and Phase Error ΔΘ

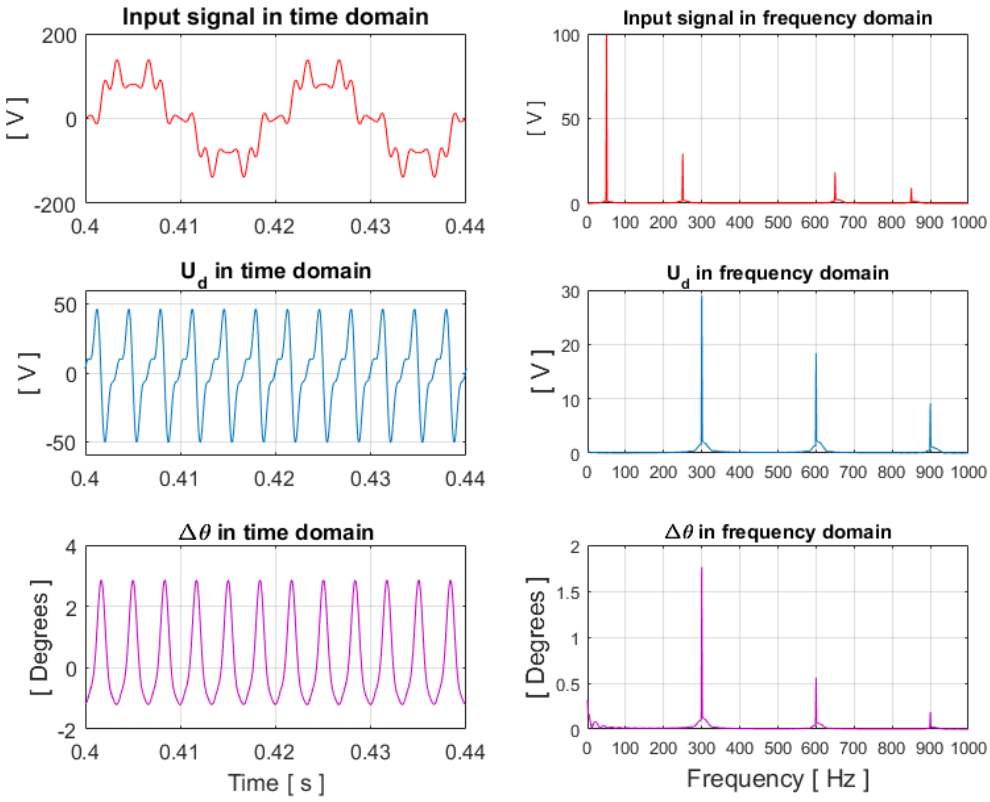


Figure 4-4: Time and Frequency Domain of the PLL Input Signal, U_d and Phase Error ΔΘ with no Harmonics Pair in the Input Signal

The PLL will deliver no oscillating values if all the harmonics contained in the input signal have the same magnitude. Likewise, an appearing harmonic in the PLL calculated values would disappear if the harmonics of the harmonics pair have the same magnitude.

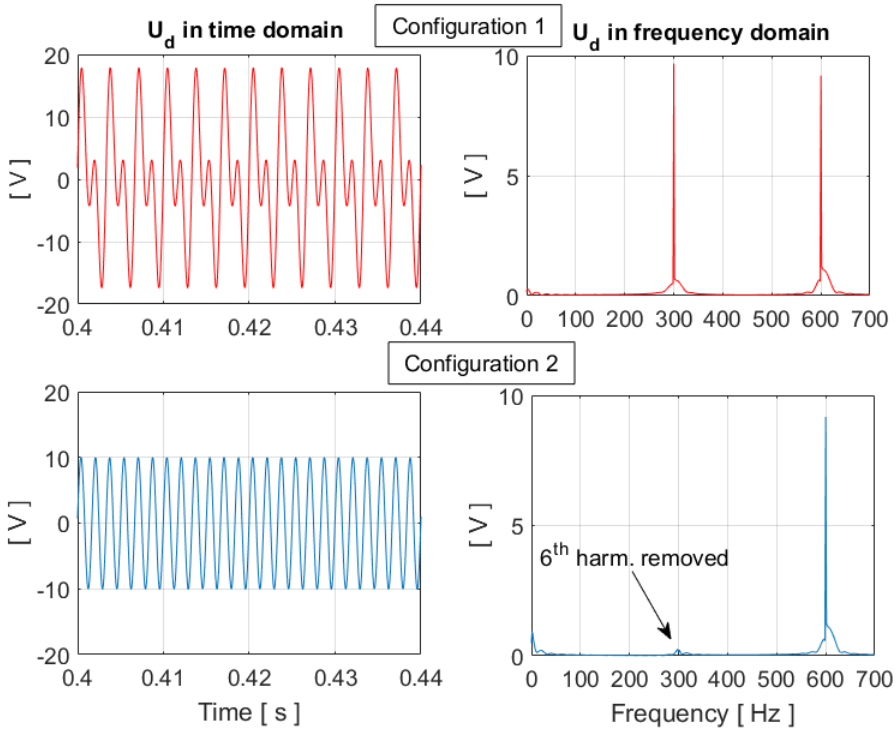


Figure 4-5: dqPLL Harmonic Rejection Due to the Input Signal Harmonics Configuration

This is shown in Figure 4-5 where the spectra of the computed direct component U_d is compared for two input signal configurations. In the first configuration, the input signal, similar to that in Figure 4-3, is a 50 Hz signal with a magnitude of 100 and is distorted by the 5^{th}, 7^{th} and 11^{th} harmonics with respectively 30V, 20V, and 10V as magnitude. In the second configuration, the magnitude of the 5^{th} and 7^{th} harmonics are both equal to 30V. As expected, the 6^{th} harmonic is cancelled out in the second configuration.

The designed dqPLL provides qualitative information about the harmonic content of the input signal. However, a further quantitive use of the delivered information that could lead to the frequency spectrum of the input voltage remains very difficult to realise due to the non-reciprocity between the observed harmonics in the values delivered by the PLL and the harmonics existing in the input signal.

4.1.2 The Instantaneous Virtual Power PLL pPLL

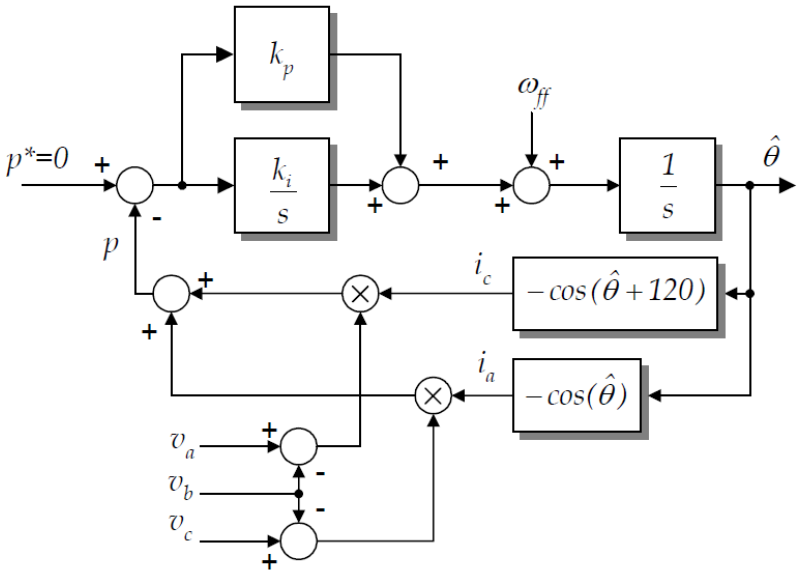


Figure 4-6: Block Diagram of the pPLL

The block diagram of the pPLL is depicted in figure Figure 4-6 [72] [73] [74]. It has similarities with the dqPLL since the estimated angular velocity is the result of a regulator. The difference here is that the controlled value is not the voltage U_d value but an imaginary instantaneous power. In order to calculate that virtual power, non-real values of currents are generated for line A and C based on the estimated phase angle assuming a balanced and harmonic free power system. The computed virtual power is the controlled value that has to be regulated to zero. The three-phase power is expressed as

$$P = v_a i_a + v_b i_b + v_c i_c \tag{4-4}$$

For current-balanced systems, $i_a + i_b + i_c = 0$ so the power can be changed to

$$P = (v_a - v_b) i_a + (v_c - v_b) i_c \tag{4-5}$$

The estimated currents are

$$\begin{cases} i_a = -\cos(\hat{\theta}) \\ i_c = -\cos\left(\hat{\theta} + \frac{2\pi}{3}\right) \end{cases} \tag{4-6}$$

With

$$\begin{cases} v_a = V \cdot \sin(\theta) \\ v_b = V \cdot sin\left(\theta - \frac{2\pi}{3}\right) \\ v_c = V \cdot sin\left(\theta + \frac{2\pi}{3}\right) \end{cases} \tag{4-7}$$

(4-6) and (4-7) into (4-5) lead to

$$P = -V\left[\left(\sin(\theta) - sin\left(\theta - \frac{2\pi}{3}\right)\right)\cos(\hat{\theta}) + \left(sin\left(\theta + \frac{2\pi}{3}\right) - sin\left(\theta - \frac{2\pi}{3}\right)\right)\cos\left(\hat{\theta} + \frac{2\pi}{3}\right)\right] \tag{4-8}$$

$$P = -\frac{3}{2} V sin(\theta - \hat{\theta}) \tag{4-9}$$

Regulating this expression to zero leads to reduce to zero the difference between the estimated phase angle and the real phase angle.

A performance evaluation has been realised in [69] and it shows that the dpPLL and the pPLL present the same dynamic response toward any input signal disturbance. The disturbances are phase jump, frequency variation, harmonic distortion and voltage unbalance. Both are sensitive to the harmonic distortion and the voltage unbalance, some derived methods have been proposed to improve the harmonic and/or the unbalance rejection [75] [76] [77] [78]. A major difference between the pPLL and the d-q PLL appears in the computational load. It is stated that the pPLL requires 46% less computing load compared to the dqPLL [69] but the dqPLL delivers more information that is useful, namely the input signal dq-frame components that can be used to calculate the magnitude and also to serve as additional control variables.

4.1.3 The Virtual Active and Reactive Power Theory PLL, pqPLL

The block diagram of the pqPLL is shown in Figure 4-7 [75]. Its working principle is based on the regulation to zero of a fictitious active power that is calculated using the transformed voltage components in the αβ-frame and the estimated current values in the same frame. The currents are assumed having an amplitude of 1, so the αβ current components are estimated to the cosine and the sine of the estimated phase angle. The controlled power value is then

$$p = v_\alpha \hat{\imath}_\alpha + v_\beta \hat{\imath}_\beta = V \cdot \cos(\theta)\cos(\hat{\theta}) + V \cdot \sin(\theta)\sin(\hat{\theta})$$
$$p = V\cos(\theta - \hat{\theta}) \qquad (4\text{-}10)$$

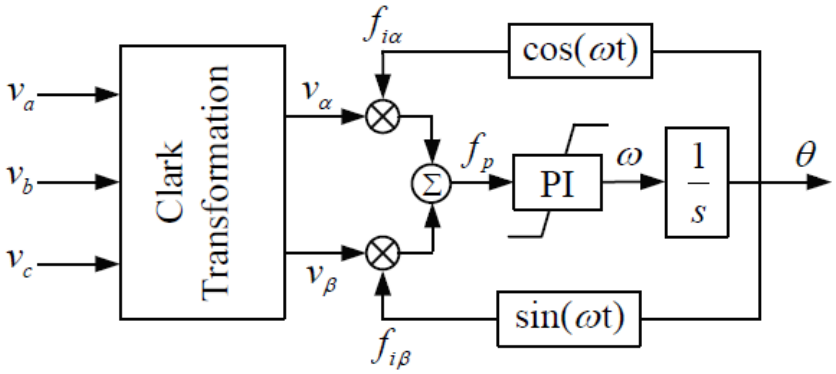


Figure 4-7: Block Diagram of the pqPLL

It has been shown that certain adverse conditions during the start-up can lead to a completely false PLL tracking. Moreover, subharmonics oscillations can make that the PLL converges to a stable point that corresponds to the subharmonic frequency [79]. The strongest feature of the pqPLL is a strong robustness even in presence of subharmonics, harmonics and negative-sequence unbalance.

4.2 The Single-phase PLLs

4.2.1 The Delay Single-phase PLL dPLL

The Figure 4-8 shows the block diagram of the single-phase dPLL [80] [81]. This one represents the least computational resources consuming PLL algorithm where a sample delay is used to build the U_β component [80]. The sample delay corresponds to one-fourth of the input signal rated period.

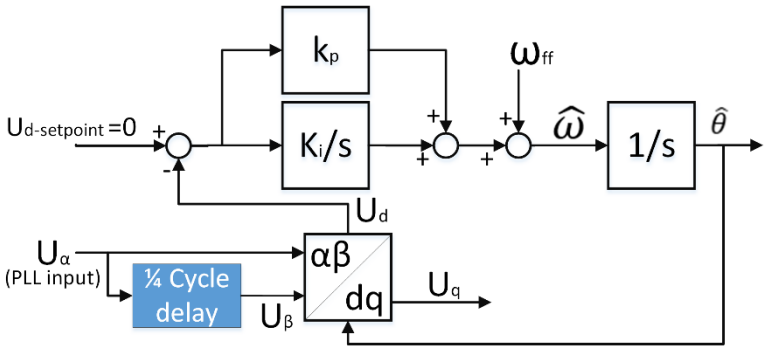


Figure 4-8: Block Diagram of the Single-phase Delay PLL – dPLL

Its major drawback is its incapacity to achieve a non-error phase angle tracking when the input signal frequency deviates from its rated frequency even if it is as robust as the dqPLL. This is due to the fixed value of the samples delay set. This causes an oscillating error on the estimated U_β- voltage component.

4.2.2 The Inverse Park Single-phase PLL – ipPLL

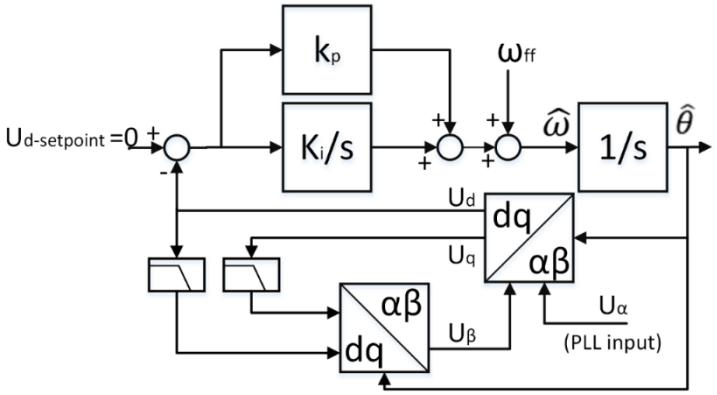


Figure 4-9: Block Diagram of the Inverse Park Single-phase PLL – ipPLL

In the case of the inverse Park PLL (ipPLL) shown in Figure 4-9 [80] [81], the quadrature U_α-voltage component is built as the feedback from the inverse Park transformation whose inputs are the synchronous voltages $U_d$and $U_q$that are filtered through first order filters [69] [82]. One important parameter is the low-pass filters. In order to avoid any impediment on the system dynamic, the filters should not have a too small bandwidth.

4.2.3 Generalized Integrator Single-phase PLL – giPLL

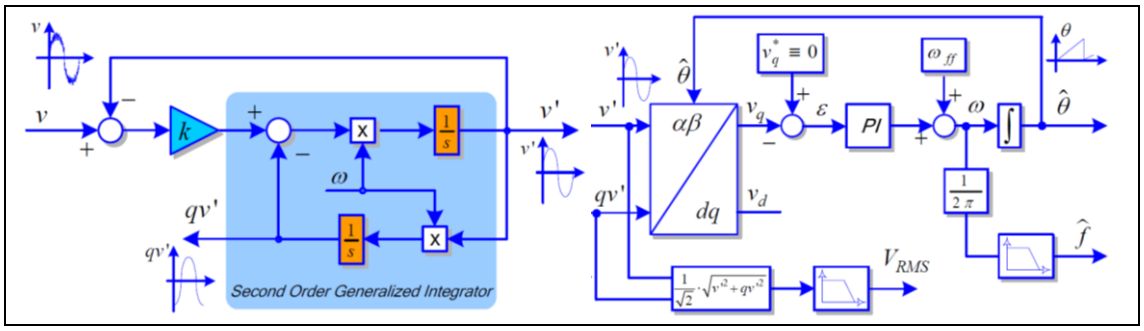


Figure 4-10: Block Diagram of the Generalized Integrator - based PLL giPLL

The Figure 4-10 depicts the $U_\alpha$voltage component generation using the second order generalized Integrator [83] [84] [85]. Two signals are generated where the first might have the same amplitude and phase as the input signal and the second signal is equal to the first but

with a phase shift of 90°. These are then used as input signals for the Park-transformation and the angular velocity controller block.

4.2.4 The Enhanced Single-phase PLL ePLL

This is one of the simplest but most complete signal identifiers. Depicted in Figure 4-11, the ePLL block diagram shows its working principle. It is a real-time reconstruction of the input signal by estimating not only the phase and frequency like in the previous PLLs but also its amplitude [86] [87]. The predominant parameter here is K, which controls the convergence speed on the estimated amplitude. The PI controller regulates the phase and the frequency estimation [76] [88]. The ePLL shows a higher immunity to the noise, the harmonics and the unbalance. Therefore, it is an effective method for the grid synchronisation and the coupling in noisy conditions [75].

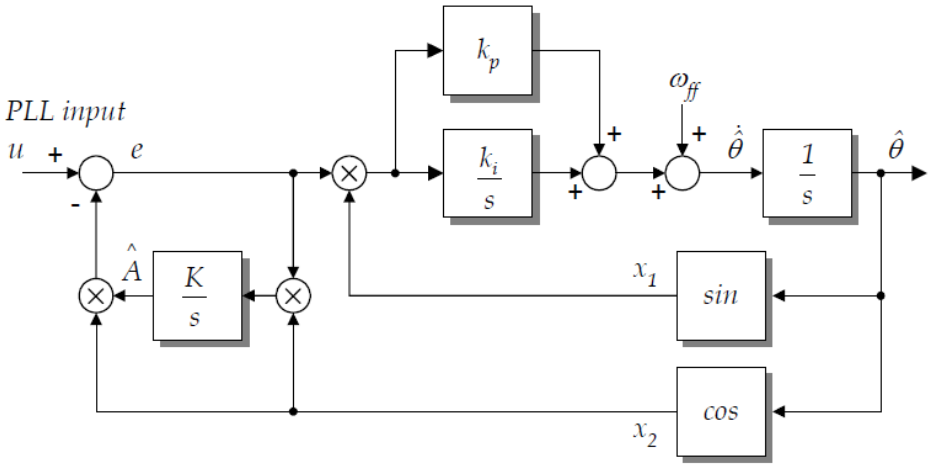


Figure 4-11: Block Diagram of the Enhanced Single-phase PLL – ePLL

Some interesting performance values can be extracted from the comparative study of the dPLL, ipPLL and the ePLL made in [89]. The computationally heaviest system is the ipPLL. This can be explained by the use of filters and the second matrix multiplication (inverse Park) for estimating the U_β- voltage component. The dPLL and the ePLL require 64% and 23% less computational load respectively compared to the iPLL. They are all sensitive to harmonics, which causes that the final estimated phase angle presents an oscillating error superimposed to a dc error. Except for the dPLL, the ipPLL and the ePLL successfully recover the phase angle error by frequency variations.

4.3 The New single-phase PLL based on the Estimated Signal Magnitude - mePLL

The accuracy and the dynamic of the single-phase park-transform based PLLs rely on how quickly and accurate the construction or estimation of the second voltage's component is in the static α-β frame. Once this second component is created, the following calculations are exactly the same as that in the 3-phase synchronous reference frame PLL (dqPLL) depicted in Figure 4-1. The following part of the chapter presents a new single-phase PLL structure, based on the same core structure as described before, but implementing a novel voltage β-component generation.

This proposed PLL tries to quickly estimate the second voltage component in the static α-β frame. On the depicted block diagram in Figure 4-12, the β-component is calculated by determining the input signal magnitude U that is then multiplied by the sinus of the estimated phase angle.

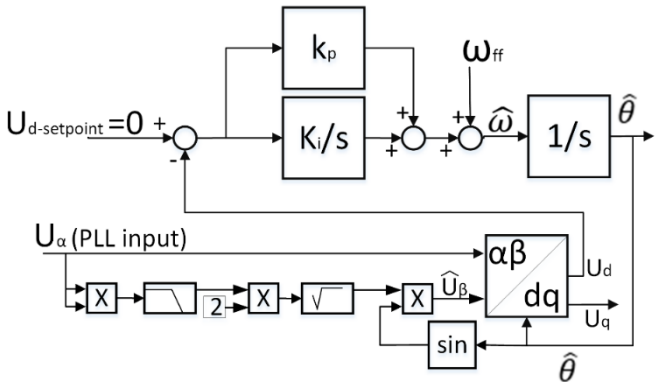


Figure 4-12: Block Diagram of the Magnitude Estimated-based PLL – mePLL

The signal amplitude is calculated as follows:

The input signal U_α, considered in a balanced system as $U \cdot cos(\omega t + \varphi)$, is squared.

$$U_\alpha^2 = [U \cdot cos(\omega t + \varphi)]^2 = \frac{1}{2}U^2(\cos(2\omega t + 2\varphi) + 1)$$
$$U_\alpha^2 = \frac{1}{2}U^2\cos(2\omega t + 2\varphi) + \frac{1}{2}U^2 \qquad (4\text{-}11)$$

This output value is oscillatory including an offset value equal to the half of the squared input signal amplitude. By the mean of a second-order low-pass filter LPF, the oscillatory part $\frac{1}{2}U^2\cos(2\omega t + 2\varphi)$ can be eliminated and the final output value of the LPF is $\frac{1}{2}U^2$. At this stage, the input signal amplitude can simply be deduced by computing the square root of the double of the LPF output value. The estimated β component is obtained by multiplying the calculated signal magnitude with the sinus of the estimated phase $\hat{\theta}$.

In order to study the system stability, this can be written in the Laplace domain.

$$U_\alpha = U \cdot cos\theta = U \cdot cos(\omega t)$$
$$\mathcal{L}(U_\alpha^2) = \mathcal{L}\left(U^2 cos^2(\omega t)\right) = \mathcal{L}\left(\frac{1}{2}U^2 cos(2\omega t) + \frac{1}{2}U^2\right) \qquad (4\text{-}12)$$

The normalized Laplace transform is

$$\mathcal{L}\left(\frac{1}{2}U^2 cos(2\omega t) + \frac{1}{2}U^2\right) = \frac{U^2}{2}\frac{2\omega \cdot s}{(s^2 + 4\omega^2)} + \frac{1}{2}U^2$$
$$= \frac{1}{2}U^2\left(\frac{s^2 + 2\omega \cdot s + 4\omega^2}{(s^2 + 4\omega^2)}\right) \qquad (4\text{-}13)$$

The transfer function of the general second order low-pass TLPF is

$$T_{LPF} = \frac{k\omega_c^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2} \qquad (4\text{-}14)$$

Because the quickest response time with no attenuation and no overshoot is required, k is set to 1 and Q to ½. This means:

$$T_{LPF} = \frac{\omega_c^2}{s^2 + 2\omega_c s + \omega_c^2} \tag{4-15}$$

The output value of the filtered squared input signal is

$$\frac{1}{2}U^2\left(\frac{s^2 + 2\omega s + 4\omega^2}{(s^2 + 4\omega^2)}\right)\left(\frac{\omega_c^2}{s^2 + 2\omega_c s + \omega_c^2}\right)$$
$$= \frac{1}{2}U^2\left[\frac{s^2 + 2\omega s + 4\omega^2}{\frac{1}{\omega_c{}^2}s^4 + \frac{2}{\omega_c}s^3 + (1 + \frac{4\omega^2}{\omega_c{}^2})s^2 + \frac{8}{\omega_c}\omega^2 s + 4\omega^2}\right] \tag{4-16}$$

Considering a 50 Hz input signal with a magnitude of 10 for example, the Figure 4-13 depicts the step response of the transfer function equivalent to the square of that input signal and the filtered output signal. The cut-off frequency of the second-order low-pass filter is set at 10Hz. It shows that the signal amplitude can be easily extracted from the filter output value. A comparison has been made concerning the response time and the oscillation cancellation efficacy of the filter depending on the cut-off frequency.

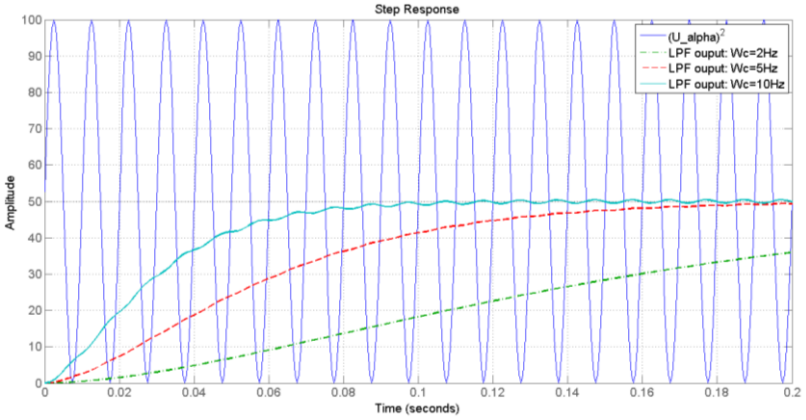


Figure 4-13: Comparison of the Low-pass Filter Output of the Squared Input Signal

It can be seen that the filtered squared value of the input signal converges, as expected, to the half of the squared of the signal amplitude. The choice of the filter cut-off frequency depends on how fast the signal magnitude needs to be determined. The faster the filter, the shorter the response time of the filter, the higher are the oscillations on the output value. As shown in Figure 4-13, the filter with the cut-off frequency set at 10 Hz needs about 80ms seconds less to reach the target value compared to the filter with a cut-off frequency at 5Hz. The one with the cut-off frequency at 2Hz is slower, reaching only about 75% of the target value after 200ms. It can be noticed that the attenuation factor of the filter increases with the input signal frequency. This means for example that the output of the same LPF will have stronger oscillations if the input frequency is 50Hz than those if the input frequency is 250Hz. It is also interesting to point out that using a LPF of a higher order with the same cut-off frequency improves the reduction of the remaining oscillations but with a longer response time. As depicted in Figure 4-14, this can be compensated by increasing the LPF to a higher order.

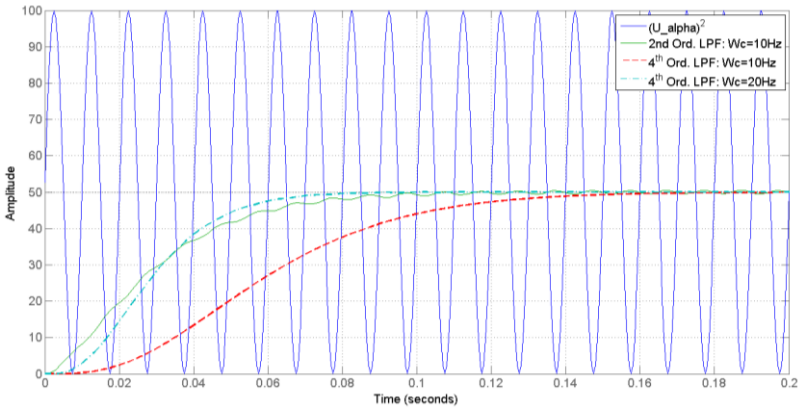


Figure 4-14: Comparison of LPFs of Different Orders and Cut-off Frequencies

Following the calculation of the voltage direct component U_d in the rotating frame through the Park transform (4-2), and replacing U_β by the calculated magnitude multiplied by the sinus of the estimated signal phase.

$$U_d = U\left[\cos\theta \sin\hat{\theta} - \sin\hat{\theta}\cos\hat{\theta}\right] \tag{4-17}$$

With $\Delta\theta = \theta - \hat{\theta}$,

$$U_d = U\left[-\frac{1}{2}\sin(\Delta\theta) + \cos\left(2\theta - \frac{3}{2}\Delta\theta\right)\cdot\sin\left(\frac{\Delta\theta}{2}\right)\right] \tag{4-18}$$

For small phase difference $\Delta\theta$, U_d can be written as following:

$$U_d = U\left[-\frac{1}{2}\Delta\theta + \cos(2\theta)\cdot\frac{\Delta\theta}{2}\right] = -\frac{1}{2}U\Delta\theta + \frac{1}{2}U\Delta\theta\cos(2\theta) \tag{4-19}$$

The voltage direct component U_d is an offset oscillatory value whose frequency is very close to the double of the input frequency and whose amplitude is proportional to the half of the input signal amplitude multiplied by the difference between the real and the estimated phases. This remains quite small especially since the difference between the real and the estimated phases is small. Regulating this voltage direct component to zero is totally possible since the amplitude of the oscillation will simultaneously decrease with the convergence of the regulated offset value ($\frac{1}{2}U\Delta\theta$) to zero.

4.3.1 The Dynamic of the me-PLL

For the stability check in the case of a frequency deviation, U_d can be considered as the sum of a non-oscillating value U_{d0} that corresponds to the offset value and an oscillating disturbance U_{dd}.

$$\begin{cases} U_{d0} = -\frac{1}{2}U\Delta\theta \\ U_{dd} = \frac{1}{2}U\Delta\theta\, cos(2\theta) \end{cases} \tag{4-20}$$

It has been shown in (4-2) that the dqPLL, whose U_d value is $U_d = -U\cdot\Delta\theta$, has the following transfer function describing the behaviour of U_d in relation to a frequency change.

$$\frac{s}{\frac{1}{U}s^2 + k_p s + k_i} \tag{4-21}$$

In this case, since the regulated value is only depending on the half of the signal amplitude, the transfer function of U_d in relation to a frequency change can directly be written as

$$TF_{U_{d0},\Delta\omega} = \frac{U_{d0}}{\Delta\omega} = \frac{s}{\frac{1}{\frac{1}{2}U}s^2 + k_p^* s + k_i^*} = \frac{s}{\frac{2}{U}s^2 + 2k_p s + 2k_i} \quad (4\text{-}22)$$

This means that the controller coefficients $k_p$and k_i should be the double of those used in a dqPLL to be able to reach the same desired dynamic. This also means that the PLL system remains stable, just like the dqPLL, as long as the controller coefficients are all positive. The ratio ${k_p}^2/k_i$ is inversely proportional to the signal amplitude; this is given by $\frac{{k_p}^2}{k_i} \geq \frac{4}{U}$.

4.3.2 Simulation Results

Using MATLAB/SIMULINK, the proposed mePLL has been built up and tested with the following parameters:

- System discrete sample rate: 20kHz
- Input signal magnitude U: 100 V
- Input signal frequency f: 250Hz
- Second order low-pass filter cut-off frequency fc: 10Hz
- PLL controller coefficients: $k_p = 2\text{rad} \cdot V^{-1}s^{-1}$, $k_i = 50\text{rad} \cdot V^{-1} \cdot s^{-2}$
- Controller feedforward angular velocity ω_{ff}: 2πf;

The simulated scenario is as follows: The PLL system runs under these conditions and after 0.3 sec, the input signal magnitude is increased by 20%. At the time 0.5 sec, a phase step variation from 0 to 15 degree occurs. Finally, a 5% relative increase of the input frequency takes place at the time 0.7 sec.

4.3.2.1 Construction of the β-component

As said before, the whole PLL performance relies on the ability to construct the second component of the voltage u_β in the stationary α-β frame. The Figure 4-15 and the Figure 4-16 show that u_β is correctly calculated and in less than 150 ms, it has already reached its final amplitude value. This response time corresponds to the LPF response time defined before (Figure 4-14). Thanks to the configured controller feedforward angular velocity, the estimated signal phase (used to compute u_β) is, if not equal, not far from the exact input signal phase. During the rising time of the magnitude of u_β the calculated rotating voltage direct component value u_d (Figure 4-17) as well as its quadrature value (not shown) and the delivered angular velocity (Figure 4-18) are oscillating but with decreasing amplitude down to zero oscillations as the magnitude of u_β grows to its final correct value.

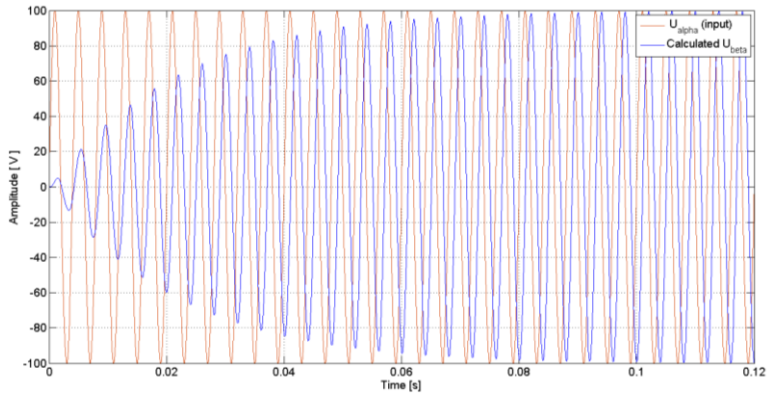


Figure 4-15: Comparison of the Input Voltage u_α and the Calculated u_β Component

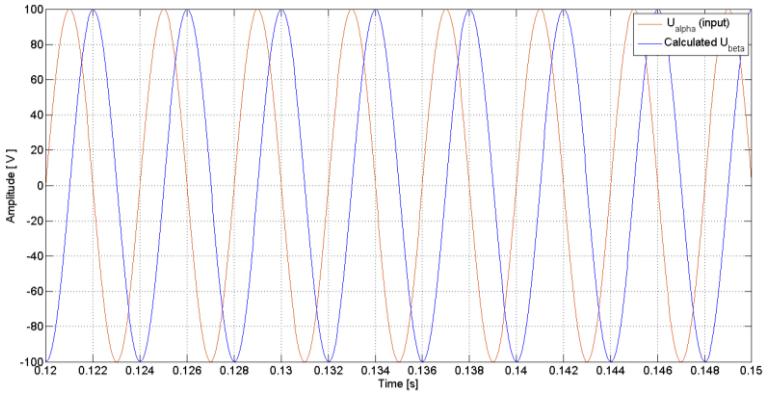


Figure 4-16: Zoomed Comparison of Input Voltage u_α and the Calculated u_β Component

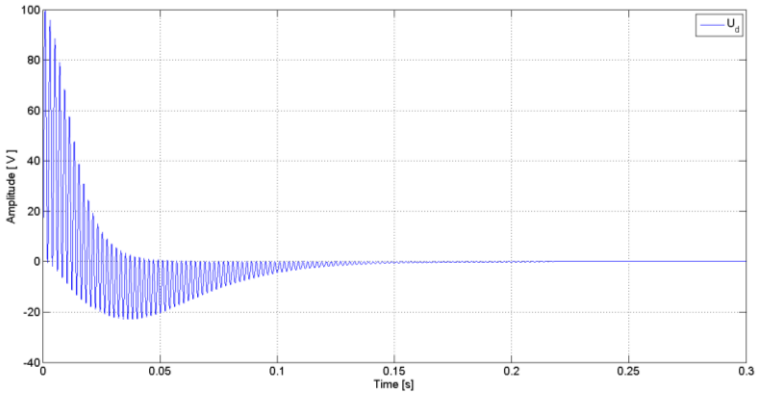


Figure 4-17: Voltage Rotating Direct Component Delivered by the mePLL

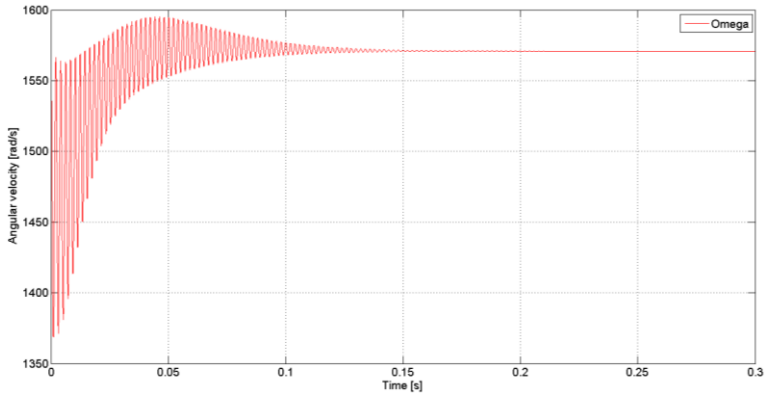


Figure 4-18: Voltage Angular Velocity Delivered by the mePLL

4.3.2.2 Input signal Magnitude Step Variation

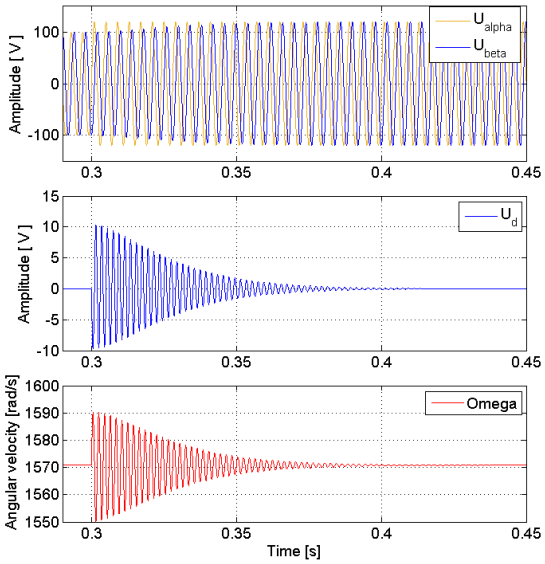


Figure 4-19: mePLL Delivered Values After an Input Signal Magnitude Jump of +20%

Here again, like at the start time of the system, the delivered values presents oscillations until the output value from the second-order LPF has reached the new signal amplitude value (Figure 4-19). So the response time here depends only on the second-order LPF dynamic. As said before, this response time can be reduced by increasing the filter order with also a higher cut-off frequency. The only constraints, in this case, are the amount of computational load, which is due to the filter and the tolerance in the amplitude determination (after the maximum oscillation amplitude on the calculated value in the transient phase).

4.3.2.3 Input signal Phase Step Variation

At time 0.5 sec, a phase step variation of +15° occurs on the input signal. The system oscillates decreasingly and finds the new operating point after about 150ms as shown in Figure 4-20. During this time the unbalance between u_α and u_β is not caused by the difference of amplitude but by the change of the input signal phase shift.

In the case of a phase step variation, the rotating direct component is calculated as follows:

$$U_d = U\left[\cos(\theta+\varphi)\sin\hat{\theta} - \sin\hat{\theta}\cos\hat{\theta}\right] \tag{4-23}$$

$$U_d = U\left[\frac{1}{2}\left(\sin(\hat{\theta}-\theta-\varphi)+\sin(\hat{\theta}+\theta+\varphi)\right)-\frac{1}{2}\sin(2\hat{\theta})\right] \tag{4-24}$$

$$U_d = U\left[-\frac{1}{2}\sin(\Delta\theta+\varphi)+\cos\left(2\theta-\frac{3}{2}\Delta\theta+\frac{1}{2}\varphi\right)\cdot\sin\left(\frac{\Delta\theta+\varphi}{2}\right)\right]$$

Assuming the PLL was already synchronized to the input signal (this means $\Delta\theta = 0$), the calculated direct component will suddenly appear oscillating with a frequency which is the double of the input frequency with a half phase step variation as phase shift. The amplitude of the oscillation is proportional to the input amplitude and the half of the phase step variation. As soon as the phase step variation occurs, the controller regulates again the voltage component u_d back to zero; this can be seen as a short impulse of the estimated angular velocity. The PLL frame accelerates to compensate the phase step variation and slows down back to the actual angular velocity value once the phase error is compensated.

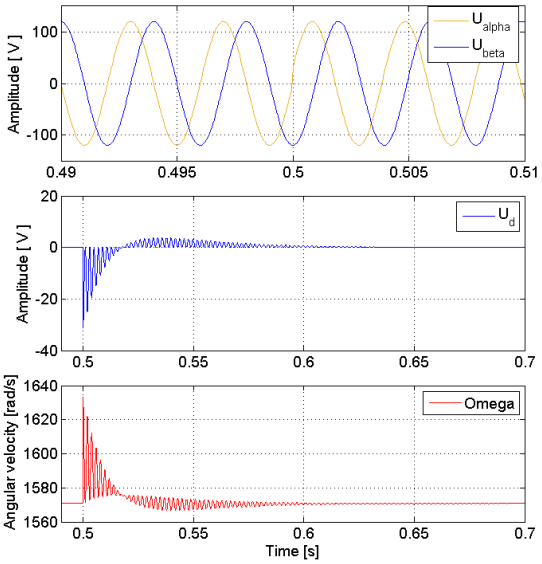


Figure 4-20: mePLL Delivered Values After an Input Signal Phase Jump +15°

4.3.2.4 Input Signal Frequency Variation

The Figure 4-21 shows how the PLL responds to a relative variation of the frequency of +5%. Still with oscillations in the transient phase, the PLL system regulates u_d back to zero, while the angular velocity value converges to the new value of the input angular velocity.

$$U_d = U\left[\cos(\theta + \varphi)\sin\hat{\theta} - \sin\hat{\theta}\cos\hat{\theta}\right] \qquad (4\text{-}25)$$
$$With\ \theta = \omega(1+\varepsilon_\omega)t = \omega t + \varepsilon_\omega \omega t, \hat{\theta} = \hat{\omega}t$$

Where $\varepsilon_\omega$represents the relative variation of the frequency/angular velocity

$$U_d = U\left[\frac{1}{2}(\sin(\hat{\omega}t - \omega(1+\varepsilon_\omega)t) + \sin(\hat{\omega}t + \omega(1+\varepsilon_\omega)t)) - \frac{1}{2}\sin(2\hat{\omega}t)\right]$$
$$U_d = U\left[\frac{1}{2}\sin(\hat{\omega}t - \omega(1+\varepsilon_\omega)t) + \frac{1}{2}\sin(\hat{\omega}t + \omega(1+\varepsilon_\omega)t) - \frac{1}{2}\sin(2\hat{\omega}t)\right] \qquad (4\text{-}26)$$
$$U_d = U\left[\frac{1}{2}\sin(\hat{\omega}t - \omega(1+\varepsilon_\omega)t) + \cos\left(\frac{3\hat{\omega}t + \omega(1+\varepsilon_\omega)t}{2}\right)\sin\left(\frac{-\hat{\omega}t + \omega(1+\varepsilon_\omega)t}{2}\right)\right]$$

Regulating U_d to zero leads to the regulation of the estimated angular velocity $\hat{\omega}$ to the new value $\omega(1+\varepsilon_\omega)$. Assuming a prior synchronization, the calculated value of U_d just after the frequency variation is

$$U\left[\frac{1}{2}\sin(-\varepsilon_\omega \omega t) + \cos\left(2\omega\left(1+\frac{\varepsilon_\omega}{4}\right)t\right)\cdot\sin\left(\frac{\varepsilon_\omega \omega t}{2}\right)\right] \qquad (4\text{-}27)$$

This maximum amplitude of the oscillation is proportional to the frequency relative deviation with a frequency equal to the double of the input signal frequency plus one-fourth of the frequency relative change. The oscillations appearing on the calculated angular frequency have the same frequency but the amplitude depends on the controller coefficients.

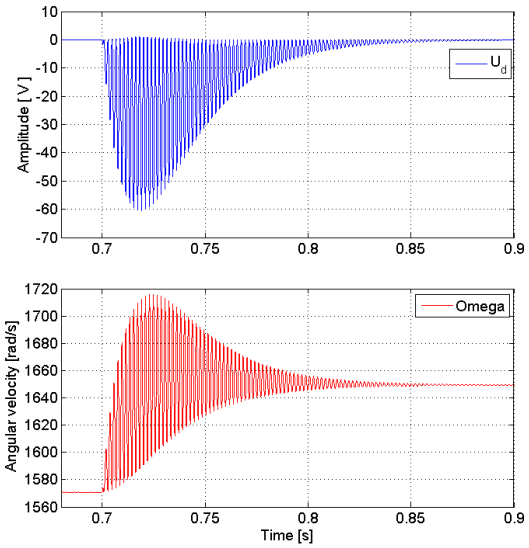


Figure 4-21: mePLL Delivered Values After a Frequency Relative Increase of 5%

4.3.2.5 mePLL Characteristic's Summary

The results obtained by the simulation show a very good behaviour of the proposed mePLL. The signal amplitude is well determined, the second stationary voltage component u_β needs a little time (corresponding to the LPF response time) to reach its final value. Despite the transitory oscillations appearing at every input signal variation, the PLL remains stable. These oscillations during the transient phase have frequencies always close to the double of the input signal frequency. Their amplitude is strongly dependent on the level (amplitude) of the variation.

If the transitory oscillations might be harmful or unwanted, it is now conceivable to filter the calculated values u_d and u_q using a band-stop filter. The band-stop filter mitigates only the oscillation due to the PLL system itself without hindering the global system dynamic (like a LPF does). Figure 4-22 shows, for example, the results obtained for the same input signal as described before and for the same mePLL but improved by filtering the output values. The band-stop filter is a second-order filter set with a nominal frequency equal to the double of the input signal (500Hz in our case).

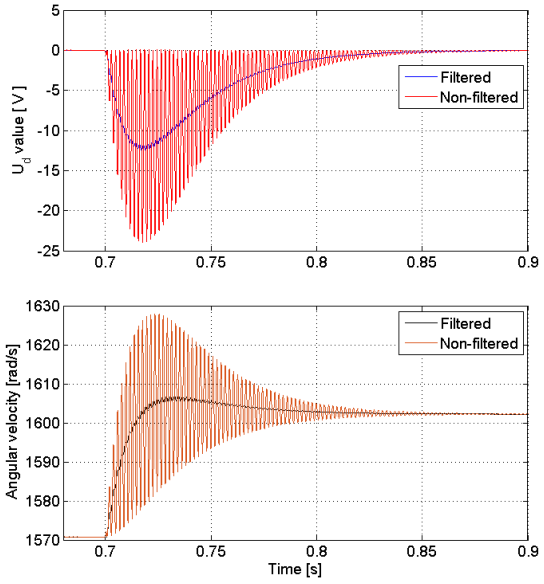


Figure 4-22: Filtered mePLL Delivered Values After a Frequency Relative Increase of 5%

4.3.3 Performance Comparison

A very good comparison point is the accuracy at which each PLL achieves the phase tracking of the input signal since the whole internal dynamic (oscillatory calculation values) can still be mitigated through filtering. Therefore, this part focuses only on the phase error realised by the compared PLLs. A first comparison is made on original, non-improved PLLs (for dPLL and mePLL). In addition, a second and last comparison gives an insight on how much the phase detection is improved.

4.3.3.1 PLLs Configuration

A 3-phase signal is generated with a frequency of 50Hz, a magnitude of 100 and no phase shift. 0.3 second later, a magnitude step variation of +20% occurs, followed by a phase step variation of +15° at the time 0.4 second. Finally, a relative frequency deviation of +2% is generated at the time 0.7 second. The dqPLL, dPLL, ipPLL giPLL and finally the mePLL have been implemented at a sampling rate of 20 kHz and the obtained values are compared. As the reference value for the angular velocity and the signal phase are given, the signal generator frequency times 2π and its integrated value respectively are measured. The dqPLL is simplified to a balanced system and it is calculated based on two voltage signals, while the others need only one input signal. They are all set to a 50Hz signal feedforward frequency and all the controllers have the same gains $\mathrm{k_p} = 1\ \mathrm{rad}V^{-1}\mathrm{s}^{-1}$ and $\mathrm{k_i} = 25\ \mathrm{rad}V^{-1}\mathrm{s}^{-2}$; except the mePLL, where they are doubled: $\mathrm{k_p} = 2\ \mathrm{rad}V^{-1}\mathrm{s}^{-1}$ and $\mathrm{k_i} = 50\ \mathrm{rad}V^{-1}\mathrm{s}^{-2}$. The sample delay by the dPLL is $100\ (1/4 \times 20\mathrm{kHz}/50\mathrm{Hz})$. The LPFs of the ipPPL have cut-off frequencies set at 50Hz. The second order generalized integrator of the giPLL has $\mathrm{k_p} = 4$ and $\mathrm{k_i} = 2 * \mathrm{pi} * 50\mathrm{s}^{-2}$. Finally, the proposed mePLL has its 6th-order IIR LPF with a cut-off frequency set at 30Hz.

4.3.3.2 Magnitude and Phase Step Variation

The Figure 4-23 and Figure 4-24 show, to the exception of the giPLL, good responses to the input signal variations. The giPLL already has a static error even at the nominal frequency. The mePLL presents a transient oscillatory period when the signal amplitude changes but quickly decays to zero. This is due to the response time of the filter used to determine the signal magnitude. The most robust PLL (but not single-phase), the dqPLL, does not show any disturbance caused by the amplitude variation. After a phase step variation, they all have the same response time, very close to that of the dqPLL, to correct the error excluding the giPLL that will keep its steady state error.

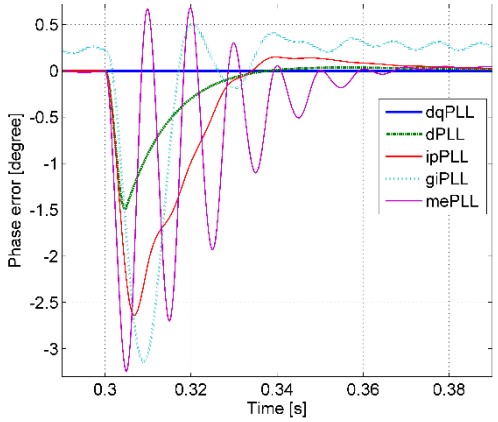


Figure 4-23: Phase Error After a Magnitude Jump of +20%

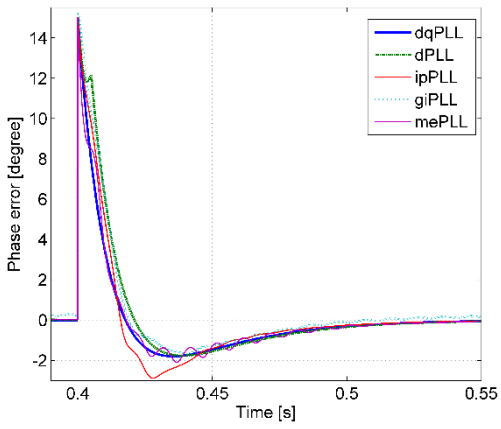


Figure 4-24: Phase Error After a Signal Phase Jump of +15°

4.3.3.3 Frequency Variation

In the case of a frequency variation (Figure 4-25), not only the giPLL but also the dPLL shows some weakness. Both have a steady phase error and that of the giPLL is still greater than its steady error before the frequency change. The proposed mePLL has a very good behaviour toward this variation despite de transitory oscillations. The oscillations are very low in magnitude and, as in the case of a magnitude and phase variation, decay quickly as the error decreases.

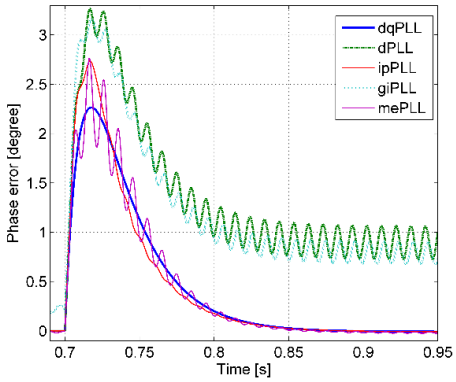


Figure 4-25: Comparison of Phase Error after a Relative Frequency Deviation of +2%

4.3.3.4 Improved mePLL

The equations (4-24) and (4-27) show that the oscillatory part in the calculated U_d value has a frequency close to the double of the signal input frequency. A band-stop filter is then used to eliminate the oscillations without hindering the system dynamic (Figure 4-26).The Figure 4-27, Figure 4-28 and Figure 4-29 show the expected improvement brought by the band-stop filters. The transitory oscillations have been eliminated and the overall calculation system remained almost unchanged in dynamic and robustness.

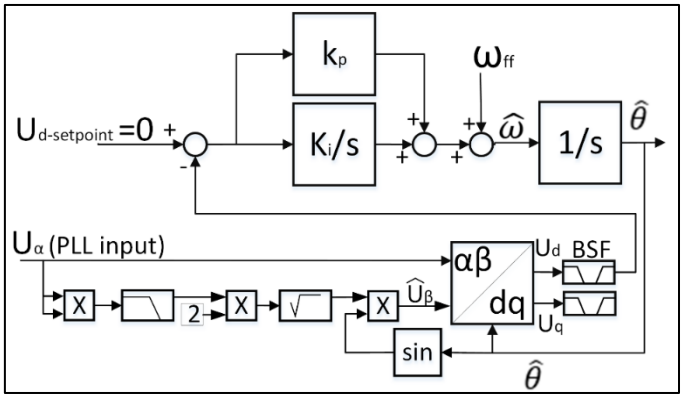


Figure 4-26: Block Diagram of the Filtered mePLL – mePLLc

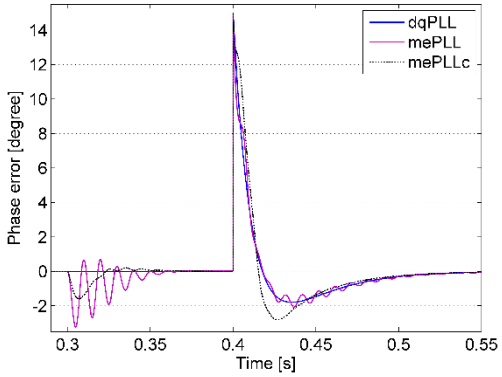


Figure 4-27: Improved Phase Error After a Magnitude Jump of +20%

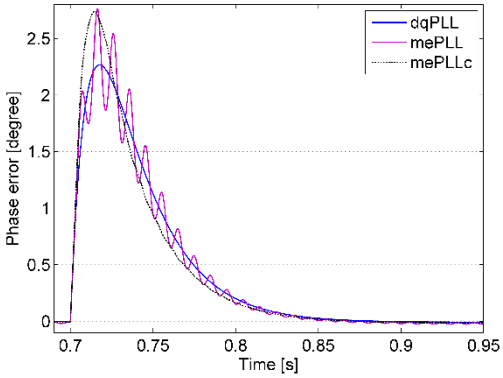


Figure 4-28: Improved Phase Error After a Phase Jump of +15°

Figure 4-30 shows the impact of the harmonics on the phase detection accuracy. In presence of the 5th harmonic (250Hz) with a relative magnitude of 40% to the fundamental, the PLL remains stable with the same dynamic but the calculated output phase position oscillates around the set point with a maximum deviation of about 2.5° and 1.5° for the mePLL and dqPLL respectively.

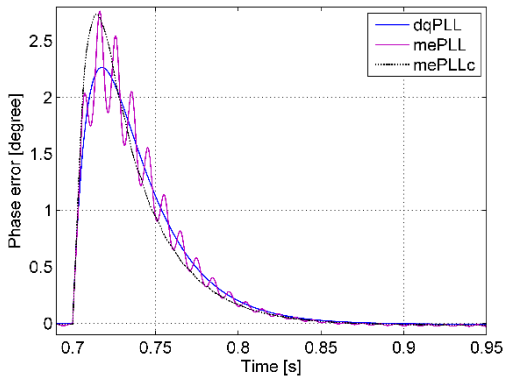


Figure 4-29: Improved Phase Error After a Relative Frequency Change of +2%

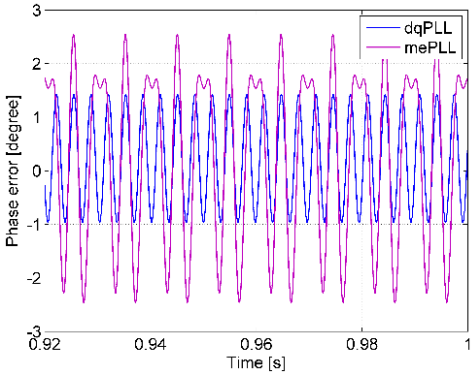


Figure 4-30: Phase Error by 40% 5th Harmonic Injection

It has been shown that the proposed new single-phase mePLL works good and accordingly to the expected mathematical equations. Comparisons made with other single-phase PLLs show its stability and reliability. The proposed structure has the following interesting properties:

- An independent magnitude output value: The calculated magnitude of the input signal does not depend on the PLL's calculations process.
- A good phase tracking even by a signal frequency change and/or harmonics presence with no phase error in steady state.
- A frequency independence compared to the dPLL where the sample delay is predefined for a given frequency and the giPLL, where the generalized integrator coefficients are also predefined for a particular frequency.

Finally, the proposed PLL structure is easy to implement and can be improved quickly (if necessary) by the mean of band-stop filters that eliminate the transitory oscillations.

4.4 Phase-error Correction of the Delay Single-phase PLL - dPLL

In 4.3.3, it has been shown that the detection efficiency of dPLL is strongly affected by the frequency changes of the input signal: An error composed of oscillations and dc offset values appears on all the calculated values. The following chapter presents how that error appears and how it can be corrected. Since its whole dynamic is the same as that of the dqPLL, a first analysis of the dqPLL detection system is realised.

4.4.1 Dynamic of the dqPLL

(4-2) shows that when the estimated phase angle $\hat{\theta}$ is nearing the real phase angle θ, U_d is approximating zero while U_q is tending to the input voltage magnitude. For a small value of $\Delta\theta = \theta - \hat{\theta}$, i.e. when the estimated phase angle is close to the real one, the direct component can be simplified as follows:

$$U_d = -U \cdot \Delta\theta$$

From the block diagram of the dqPLL (Figure 4-1), it can be written:

$$-U_d = U(\omega t - \hat{\omega} t)$$

$$U_d = U\left(\frac{\omega}{s} - \frac{\hat{\omega}}{s}\right) = U\left(\frac{\omega}{s} - \frac{1}{s}\left(\omega_{ff} + \left(k_p + \frac{k_i}{s}\right)\cdot(-U_d)\right)\right)$$

$$\begin{cases} U, U_d \; in \; V \\ \omega, \omega_{ff} \; in \frac{rad}{s} \\ k_p \; in \frac{rad}{V \cdot s} \\ k_i \; in \frac{rad}{V \cdot s^2} \end{cases}$$

$$With \; \Delta\omega = (\omega_{ff} - \omega), \qquad U_d = \frac{\Delta\omega \cdot s}{\frac{1}{U}s^2 + sk_p + k_i}$$

The transfer function describing the evolution of U_d in function of the frequency/angular velocity variation of the input signal is therefore:

$$TF_{U_d,\Delta\omega} = \frac{U_d}{\Delta\omega} = \frac{s}{\frac{1}{U}s^2 + sk_p + k_i} \qquad (4\text{-}28)$$

Therefore, the transfer function linking the estimated angular velocity and a frequency deviation from the feed-forward frequency is

$$TF_{\hat{\omega},\Delta\omega} = \frac{-sk_p - k_i}{\frac{1}{U}s^2 + sk_p + k_i} \qquad (4\text{-}29)$$

Since U is necessarily positive and following the Routh stability criteria, the system will be stable when the regulator k_p and k_i are positive. The dynamic and robustness are determined by the value of the coefficients. The boundary condition to no overshoot is given by

$$k_p^2 - \frac{4k_i}{U} \geq 0 \rightarrow \frac{k_p^2}{k_i} \geq \frac{4}{U} \qquad (4\text{-}30)$$

The ratio ${k_p}^2/k_i$ is then inversely proportional to the signal magnitude. This means, to maintain de same robustness of the system, the controller coefficients ratio k_p to k_i has to increase by decreasing magnitude and inversely. This gives the idea of implementing an adaptive controller especially in the case of a harmonic compensation system where the harmonic's magnitude is decreasing to zero. Adapting the coefficient can be done until a given acceptable lowest harmonic magnitude. At that point, phase angle errors due to long response time of the PLL may not noticeably affect the overall compensation process.

4.4.2 Dynamic of the dPLL

The error appearing in the dPLL calculations comes from the approximate estimation of the β-component of the voltage, which is then used by the dq-transformation. The fixed number of samples chosen for the delay corresponds to a quarter of the period of the input signal at the rated frequency. Assuming $U_\alpha = U\cos\omega t$, to build up the U_β component,

$$U_\beta = U_\alpha\left(t - {}^1/_4\, T_0\right) = U\cos\left(\omega\left(t - {}^1/_4\; T_0\right)\right) \qquad (4\text{-}31)$$

Where: ω is the actual angular velocity and T_0 the rated time period.

U_β can also be written using the rated angular velocity ω_0 as

$$U_\beta = U\cos\left(\omega t - \frac{\pi}{2}\frac{\omega}{\omega_0}\right) \quad (4\text{-}32)$$

With $\omega = \omega_0(1+\varepsilon_\omega)$ where ε_ω represents the relative variation of the angular velocity.

$$U_\beta = U\cos\left(\omega t - \frac{\pi}{2}(1+\varepsilon_\omega)\right) \quad (4\text{-}33)$$
$$\rightarrow U_\beta = U\sin(\omega t - \frac{\pi}{2}\,\varepsilon_\omega)$$

Using the dq-transformation matrix (4-1), the direct voltage component in the dq-frame can be written as follows:

$$U_d = U\left[\cos(\theta)\sin(\hat{\theta}) - \cos(\hat{\theta})\,\sin(\theta - \frac{\pi}{2}\,\varepsilon_\omega)\right] \quad (4\text{-}34)$$

$With\ \Delta\theta = \theta - \hat{\theta}\ and\ \alpha = \frac{\pi}{4}\,\varepsilon_\omega$ then:

$$U_d = U\left[\frac{1}{2}\sin(-\Delta\theta) - \frac{1}{2}\sin(-2\alpha + \Delta\theta) + \frac{1}{2}(2\cos(2\theta - \Delta\theta - \alpha)\sin(\alpha))\right] \quad (4\text{-}35)$$

Since $\Delta\theta$ and α are very small values, U_d can be approximate as:

$$U_d \approx U(-\Delta\theta + \alpha) + U\cdot\alpha\cos(2\theta - \Delta\theta - \alpha) \quad (4\text{-}36)$$

This means, U_d has an oscillatory part U_{dd} equal to $U\cdot\alpha\cos(2\theta - \Delta\theta - \alpha)$ whose frequency is very close to the double of the input signal frequency and its magnitude $U\cdot\alpha$ is proportional to the input signal magnitude U and the relative variation of the input signal frequency to the rated frequency. This oscillatory part is considered as measurement disturbance to the stationary part U_{d0}.

$$U_{d0} = -U\cdot\Delta\theta + U\cdot\alpha \quad (4\text{-}37)$$

$$U_{d0} = -U\left(\frac{\omega}{s} - \frac{1}{s}\left(\omega_{ff} + \left(k_p + \frac{k_i}{s}\right)\cdot(-U_{d0})\right)\right) + U\cdot\alpha \quad (4\text{-}38)$$

$$U_{d0} = \frac{(\omega_{ff} - \omega)s + \alpha s^2}{\frac{1}{U}s^2 + (sk_p + k_i)} \quad (4\text{-}39)$$

$$with\ \Delta\omega = \omega_{ff} - \omega\ and\ \alpha = \frac{\pi}{4}\frac{\omega - \omega_{ff}}{\omega_{ff}} = -\frac{\pi}{4}\frac{\Delta\omega}{\omega_{ff}} = A\cdot\Delta\omega$$

$$\frac{U_{d0}}{\Delta\omega} = \frac{As^2 + s}{\frac{1}{U}s^2 + k_p s + k_i} \quad (4\text{-}40)$$

The characteristic equation of the transfer function is the same as the one for the dq-PLL; this means the dPLL has exactly the same dynamic and robustness as the dqPLL: the U_β calculation using the samples delay cannot lead to the instability of the PLL system but to an inaccuracy. When the frequency of the input signal is equal to the nominal frequency of the PLL, $\alpha = 0$ this induces $U_{dd} = 0$ and $U_{d0} = -U\Delta\theta$. The dPLL in the case of no frequency deviation has exactly the same results as the dqPLL.

4.4.3 Phase Error Correction Methods

The non-oscillatory expression of the voltage direct component given in (4-37) shows that applying the standard U_d regulation to zero will automatically lead to a steady phase-shift that is equal to α.

$$-U\Delta\theta + U\alpha = 0 \rightarrow \Delta\theta = \alpha \qquad (4\text{-}41)$$

To avoid this permanent error on the signal phase position, one can choose to

- Change the PI controller set-point to $U \cdot \alpha$
- Correct the final output phase position by an offset α
- Prevent the appearance of the phase-shift

4.4.3.1 Delay PLL with Modified PI Controller's Set-point– dPLL-Csp

The block diagram depicted in Figure 4-31 shows the structure of a delay PLL where the regulator set-point is not zero. The main idea of this method is to regulate the U_d value to another set-point U_{d-sp} inducing a zero-error estimated angle. Based on (4-41), it can be observed that changing the set-point from zero to $U \cdot \alpha$ automatically leads to regulating the phase error to zero. Normally, the input signal amplitude U and the relative frequency deviation from the rated frequency are unknown (used to calculate α). However, the PLL itself, despite the oscillatory output values, gives good indicators of these unknown values: the quadrature component U_q is very close to the signal amplitude so is also the estimated angular velocity to the real one therefore the estimated relative angular velocity change. Therefore, the regulator set-point is given by

$$U_{d-sp} = U_q \cdot \hat{\alpha} \; where \; \hat{\alpha} = \frac{\pi}{4}\widehat{\varepsilon_\omega} = \frac{\pi}{4}\left(\frac{\hat{\omega} - \omega_{ff}}{\omega_{ff}}\right) \qquad (4\text{-}42)$$

This method focuses only on the offset value α; this means there will be a remaining oscillatory part appearing in the final output angle position since there is no correction for it.

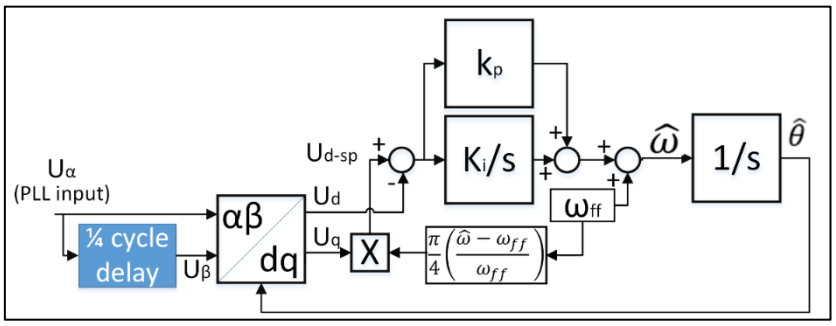


Figure 4-31: Block Diagram of the Delay PLL with Modified Controller Set-point

4.4.3.2 Delay PLL with Corrected Output Angle – dPLL-Ca

Very similar to the dPLL-Csp, this structure (Figure 4-32) focuses on correcting the final output angle without changing the U_d regulator set-point. In this case, the correction has absolutely no impact on the system computations since the correction is only for the final output value with no feedback loop. Our goal being to make sure that the PLL is in phase with the input signal, this means no difference between the actual phase and the adjusted estimated phase $\hat{\theta}_c$ by the PLL.

$$\theta - \hat{\theta}_c = 0$$

However, we know from (4-41) that there is a systematic error α

$$\theta - \hat{\theta} = \hat{\alpha}$$

So the final output phase angle is corrected as

$$\hat{\theta}_c = \hat{\theta} + \hat{\alpha} \;\; with \; \hat{\alpha} = \frac{\pi}{4}\frac{\left(\hat{\omega} - \omega_{ff}\right)}{\omega_{ff}} \tag{4-43}$$

Just like the previous method, this will correct only the offset value α ignoring the oscillations.

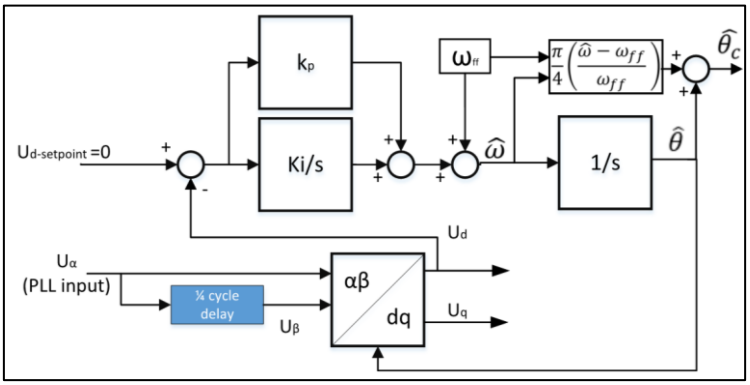


Figure 4-32: Block Diagram of the Delay PLL with the Corrected Output Phase-angle Value

4.4.3.3 Delay PLL with Corrected Voltage β-component – dPLL-CUb

Any variation of the input signal frequency from the rated PLL frequency causes oscillating errors on the delivered values. This is due to the fixed length delay set for the rated frequency, which causes a bad estimation of the voltage component U_β. The two previous methods focus on correcting the consequences of the bad estimation of U_β in the contrary of the following method (Figure 4-33) that concentrates on avoiding the error in the estimation of U_β.

(4-33) gives the expression of U_β directly determined through the transfer delay $U_{\beta 0}$

$$\begin{aligned} U_{\beta 0} &= U\sin(\omega t - \frac{\pi}{2}\,\varepsilon_\omega) \\ U_{\beta 0} &= U\sin(\omega t)\cos\left(\frac{\pi}{2}\,\varepsilon_\omega\right) - U\cos(\omega t)\sin\left(\frac{\pi}{2}\,\varepsilon_\omega\right) \\ U_{\beta 0} &= U\sin(\omega t)\cos\left(\frac{\pi}{2}\,\varepsilon_\omega\right) - U_\alpha\sin\left(\frac{\pi}{2}\,\varepsilon_\omega\right) \end{aligned} \tag{4-44}$$

In order to have the corrected error-free value $U_{\beta c}$ of U_β which should be $U\sin(\omega t)$, $U_{\beta 0}$ should be corrected to

$$U_{\beta c} = \frac{U_{\beta 0} + U_\alpha \sin\left(\frac{\pi}{2}\,\varepsilon_\omega\right)}{\cos\left(\frac{\pi}{2}\,\varepsilon_\omega\right)} \tag{4-45}$$

Exactly the same way as in the two previous cases, the estimated relative frequency variation is used since the exact value is unknown.

$$U_{\beta c} = \frac{U_{\beta 0} + U_\alpha \sin\left(\frac{\pi}{2}\,\widehat{\varepsilon_\omega}\right)}{\cos\left(\frac{\pi}{2}\,\widehat{\varepsilon_\omega}\right)} \tag{4-46}$$

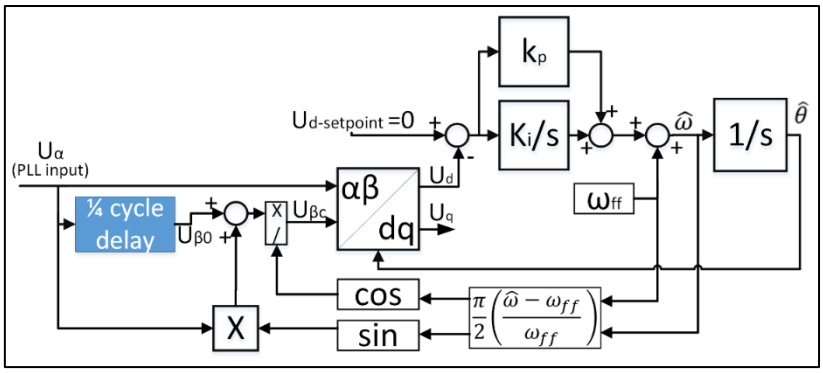


Figure 4-33: Block Diagram of the Delay PLL with the Corrected θ-Component

4.4.3.4 Performance Evaluation

A 3-phase signal is generated with a frequency of 50Hz, a magnitude of 100 and no phase shift. 0.3 second later occurs a magnitude step variation (a voltage swell) of +20%, followed by a phase step variation of +15° at the time 0.4 second finally occurs a relative frequency deviation of +2% at the time 0.7 second. As reference value for the angular velocity and signal phase is taken the signal generator frequency times 2π and its integrated value respectively. The tested PLLs are all set for a 50Hz signal (feedforward frequency), all the controllers have the same gains $\mathrm{k_p} = 1\ \mathrm{rad}V^{-1}\mathrm{s}^{-1}$ and $\mathrm{k_i} = 25\ \mathrm{rad}V^{-1}\mathrm{s}^{-2}$ and the sample delay length is $100\left(\frac{1}{4}\cdot\left(\frac{20\ kHz}{50\ Hz}\right)\right)$. They are also compared to the results delivered by the dqPLL taken as correct reference result on which their main structured is based.

4.4.3.4.1 Magnitude and Phase Step Variation

Figure 4-34 shows the evolution of the phase-error caused by a swell of 20%. All the PLLs (single-phase) except the dqPLL (3-phases) exhibits a phase error between 1.5 and 2.5 degrees. On the one hand, this error is rapidly reduced within 20ms down to less than 0.2 degree. On the other hand, a 15° phase-shift of the input signal has nearly the same impact on all the PLLs that need about 100ms to get the phase-error under 0.5 degree (Figure 4-35). These observations show that the different changes made in the dPLL structures do not affect the dynamic response to the input signal amplitude and phase variation.

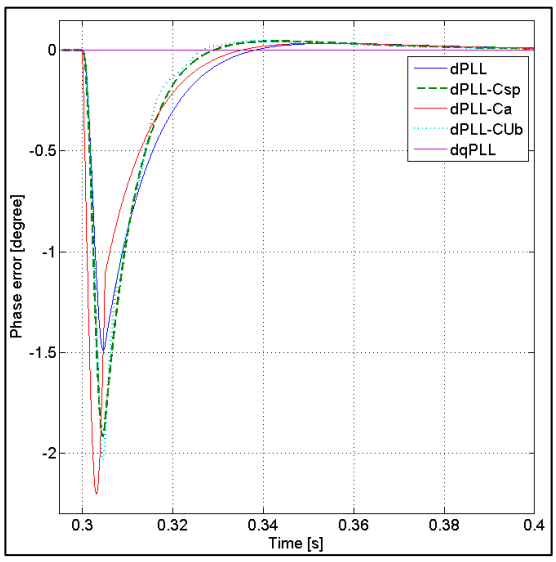


Figure 4-34: PLLs Phase-angle Response to a Voltage Swell of +20%

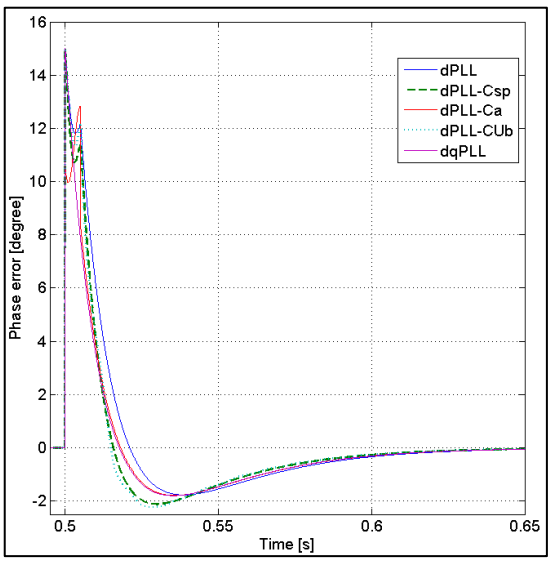


Figure 4-35: PLLs Phase-angle Response to a Phase-jump of +15°

4.4.3.4.2 Frequency Variation

The main weakness of the standard dPLL is depicted in Figure 4-36: any frequency deviation from its rated frequency leads to a steady oscillating phase-error. The realised modifications worked as expected. The improvement brought by the dPLL-Csp as well as the dPLL-Ca is the cancellation of the steady error despite the increase of the magnitude of the oscillations. However, the magnitude of the oscillations remains very small (about 0.25 and 0.35 degree for dPLL-Csp and dPLL-Ca respectively). The best correction is performed by the dPLL-Cub where not only the steady offset error but also the oscillations disappear. It can also be observed that all the PLLs including the reference dqPLL have the same response time to reach their final value.

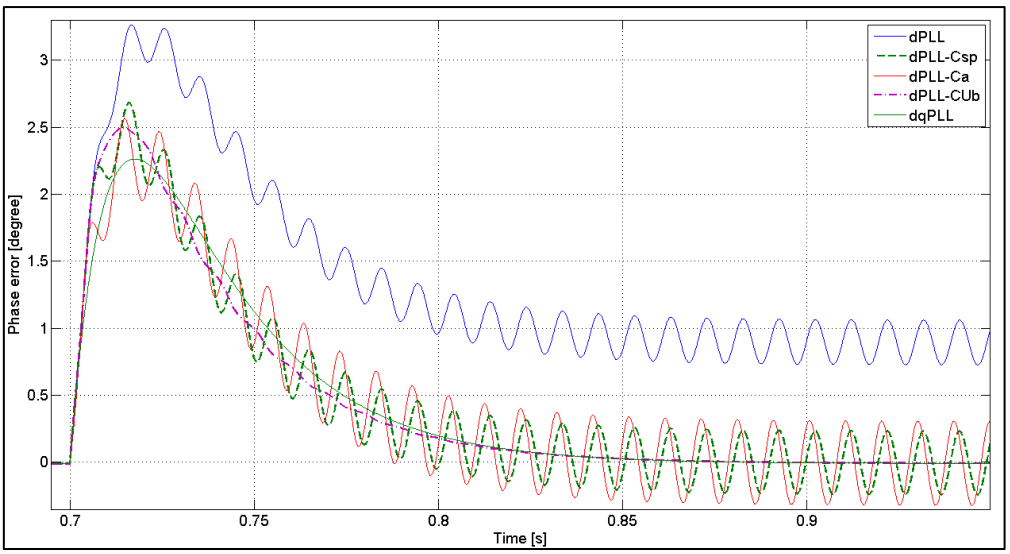


Figure 4-36: Phase-angle Response to a Frequency Increase of 2%

The Figure 4-37 shows the evolution of the maximum magnitude of the oscillating phase errors after the 5th harmonic is injected, with different magnitudes, into the input signal. First, this reveals that no PLL is immunised against the harmonics with the dPLL-Ca having the highest sensitivity. The dPLL-CUb is more accurate than the other single-phase PLLs with no harmonics present. However, it becomes very quickly less accurate than the dPLL-Csp by increasing harmonic level. Filtering the control value U_d for the dPLL-Csp and the dPLL-Ca with band-stop filters (since the oscillations frequency range or the output error is known and is very close to the double of the input frequency - (4-31) brings considerable ameliorations. As shown on Figure 4-38, the phase-error is no longer oscillating and is zero for a harmonic-free signal. Their sensitivity is reduced by around 34% and 54% respectively. The fact that the filtered dPLL-Csp depicts a better accuracy than the dqPLL when dealing with distorted input signals may not be seen as a better result because the filter added to the dPLL-Csp reduces also the harmonics amplitude whose frequency is included in the bandwidth of the band-stop filter.

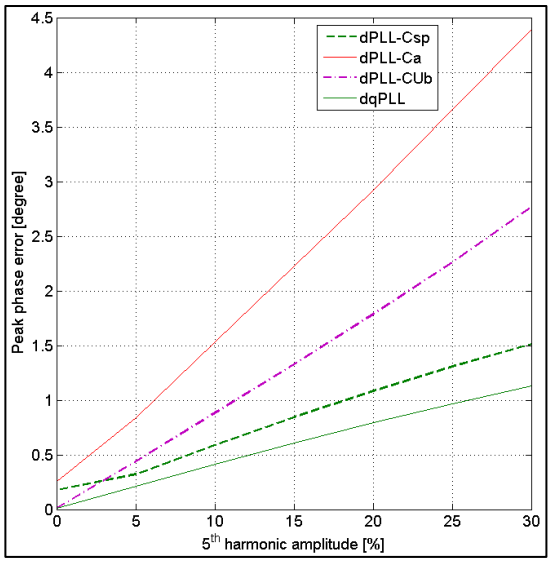


Figure 4-37: PLLs Peak Phase Error in Function of 5th Harmonic Amplitude

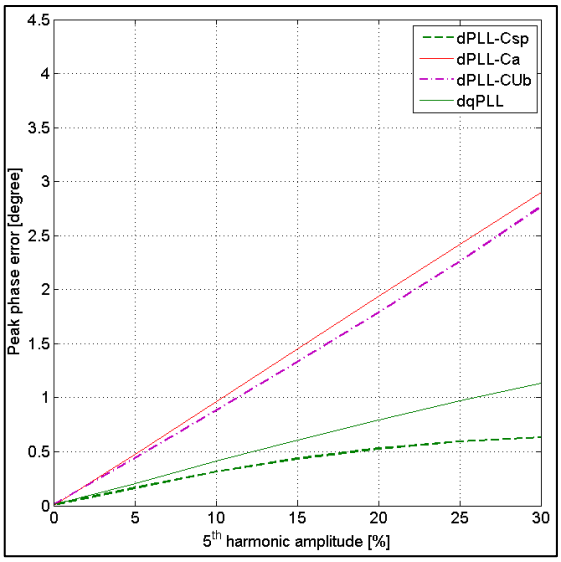


Figure 4-38: Filtered PLLs Peak Phase Error in Function of the 5th Harmonic Amplitude

The structures dPLL-Ca and the dPLL-Csp for the error mitigation succeed in cancelling the offset error but not the oscillations while the error-preventing structure dPLL-CUb eliminates also the oscillations. The proposed structures also proved their good performances in presence of harmonic disturbances in the input signal. Filtering the output voltage direct component U_d for dPLL-Ca and dPLL-Csp improves considerably not only their correction efficiency but also cancel the oscillations and reduce their sensitivity to the harmonic distortion in the input signal. This makes the dPLL-Csp even less sensitive to disturbances than the robust dqPLL.

4.5 Conclusion

There are so many different PLL algorithms that for every application type, the most suitable method can be found. A large number of the existing PLLs have the same basic principle but some are modified versions designed to achieve better results such as a better rejection of the harmonics or the load unbalance. Similarly, to the harmonic detection methods for APFs, the computational load is increasingly becoming the least important constraint due to the progress in the micro-controllers. So many applications have the tendency to implement more powerful PLLs that incorporate every good performance indicators such as the rejection of the harmonics and the load unbalance.

5 Selective Active Power Voltage Filter Based on FIR-Filter

The previous chapters have shown the different topologies of APFs and different harmonic detection algorithms already existing. The following part presents a new APF topology for the compensation of voltage harmonics based on a voltage source inverter (VSI) with a particular focus on the harmonics detection and compensation technique. The system is simulated in SIMULINK and then implemented on a test rig in the lab for validation.

5.1 System Topology

The Figure 5-1 depicts the topology of the developed APF, which is very close to a series APF as described in paragraph 2.2. The particularity here relies on the interaction interface between the power grid and the controlled VSI. The 3-phase VSI output voltage as a pulse width modulated voltage is filtered using a passive parallel LC low-pass filter that is able to filter the voltage harmonics down to 1 kHz only. The sinusoidal output voltage of the filter is finally synchronized and coupled with the existing AC power source. The compensation of the existing harmonic in the main AC power voltages results in generating, with the VSI, the opposite voltage signals of the existing and measured harmonics.

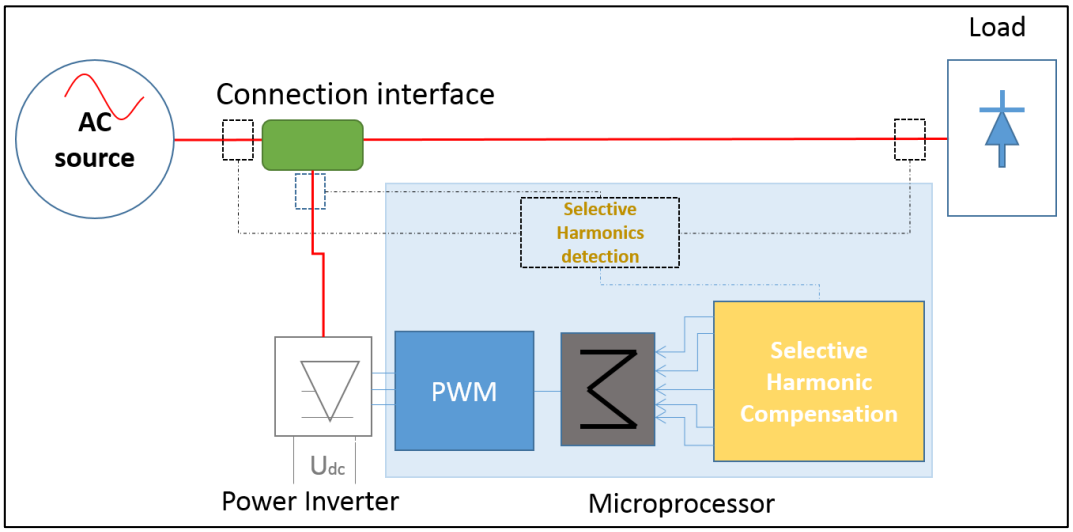


Figure 5-1: Topology of the Inverter as a Shunt and Selective APF

On the one hand, this topology gives to the APF the following tremendous advantages:

- In order to compensate the voltage harmonics, most of the APFs work on compensating firstly the currents, then by a feedback effect, the compensated currents depicting an almost perfect sine waveform will have no impact on the voltage waveforms which will then be almost harmonic free. This APF topology allows working directly on the voltage waveform without having to work on the ones of the currents.
- Since the whole APF system can be considered as a secondary parallel power source, it can also be used for supporting the main power source by injecting or absorbing the active or reactive power in or from the main grid.
- The APF can be used as a harmonic auto-compensated voltage source. In case of interruption of the power from the main grid or also for off-grid operations, the APF is able not only to generate itself a local grid with the same characteristics as the main

(but unavailable) power grid but also to eliminate the eventual harmonics when any non-linear load is connected.

- This can work for single phase as well as 3-phase power systems.

On the other hand, one aspect that can be considered as a drawback is that the APF cannot be used if the DC voltage level on the DC link of the VSI is not high enough to generate the fundamental wave for a grid-tied as well as for an off-grid operation. This means for example that, if the DC voltage level falls down to 200V, whose source might be a battery bank fed by a renewable energy source like a photovoltaic system or a wind turbine, the complete compensation will stop since at least 400V is required. However, this 200V would have been enough to mitigate some harmonics if another APF topology was used.

5.2 Harmonics Detection and Compensation Method Based on PLLs

The proposed method, a selective detection and compensation methodology based on the Fourier principle, which stipulates that every periodic function can be represented as a superposition of several sinusoidal functions. Each single voltage frequency is treated (magnitude and phase angle detection) individually and simultaneously and after every harmonic compensation and the fundamental control voltage is rebuilt, they are all added together to form the final voltage value that is then forwarded to the VSI PWM control. The closed-loop control of the fundamental frequency and the harmonics for a 3-phase system is shown in Figure 5-2.

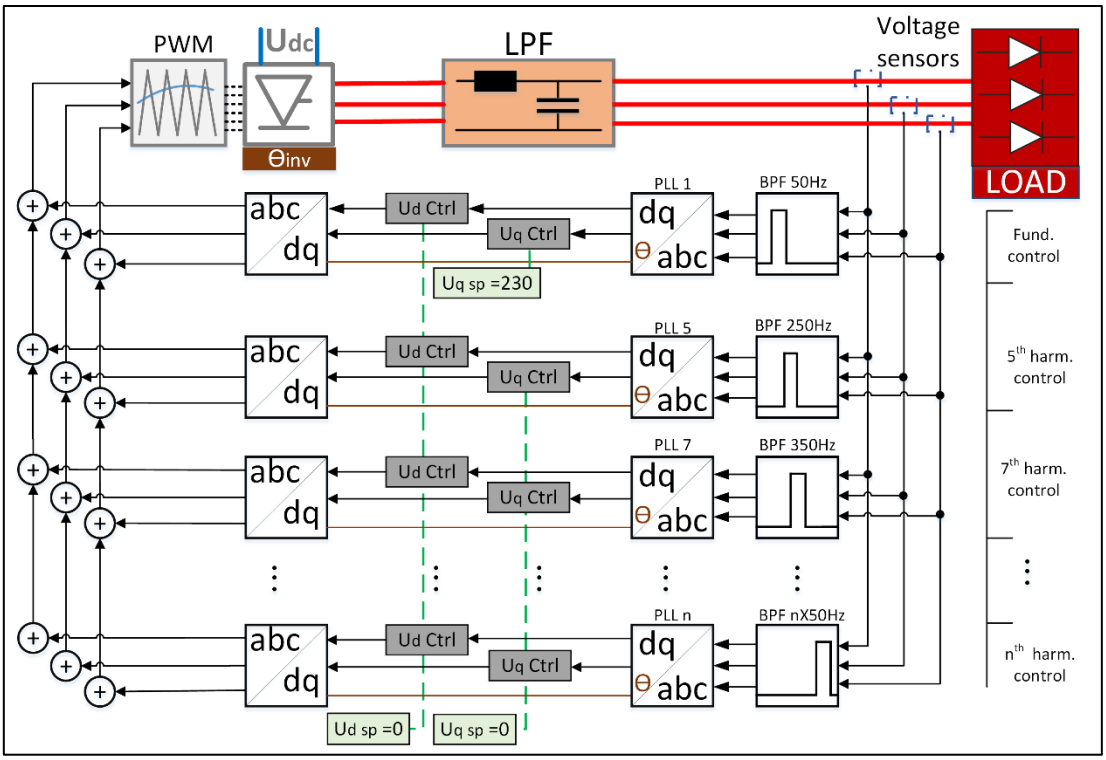


Figure 5-2: Closed Loop Diagram of the Selective FIR filter and PLL-based Harmonic Compensation

Here are the consecutive steps for the control:

- Signal decomposition: FIR band-pass filters are used to extract from the raw voltages signals (measured at the point of common coupling PCC) only the targeted frequencies. This represents the waveform decomposition step.

- Harmonic signal identification: Once every signal is separated from the others, a signal identification occurs. A 3-phase SRF-based PLL is applied to decompose the 3-phase voltage system into the 2-axis orthogonal and rotating dq-frame, which is basically the transformation of AC values in a stationary frame into DC values in a rotating frame. This step provides the phase angle of the signal and its corresponding DC voltage components u_d and u_q values (at that phase position).
- Harmonic signal magnitude control: PI controllers are used for controlling the magnitude of the signal by controlling the u_d and u_q values. These values are controlled to zero for every considered harmonic and in case of the stand-alone operation, where the fundamental voltage also has to be generated, the fundamental U_d value is regulated to zero while its U_q value is regulated to the standard fundamental magnitude (RMS value: 230V +- 10%). In the grid tied situations, the fundamental control will be executed only during the synchronisation step, where its amplitude will be regulated to that of the main power grid. After the synchronisation and coupling, the active and reactive power become the controlled values.
- Control and compensation signal generation: the output values of each harmonic PI controller constitutes the compensation voltage components in the dq-frame. These compensation values are transformed back to the 3-phase system by applying the inverse Park transform using the phase angle determined by the PLL and then the Inverse Clarke transform. For the fundamental in the off-grid situation, its controller output values are not compensatory, since they do not tend to reduce its amplitude to zero. In grid-tied operation, the fundamental control values will not be generated by the controller of these voltage's dq components but by the controllers of the fundamental power transfer.
- Reconstruction of the final voltage value: all the 3-phase values (the harmonics compensation voltages plus the fundamental voltage) are summed together to make the instantaneous final voltage value.
- VSI control and 3-phases voltage generation: Using the final instantaneous value generated before, the firing signals for the VSI are released based on the method of the triangle-sinus wave comparison (see 5.3.4.1). The PWM voltages containing the distorted compensation voltage right at the output terminals of the VSI are finally sent through the passive low-pass LC filter. The superimposed generated distortion and the load-induced distortion cancel each other at the PCC, the voltages are measured again and so the control loop is closed.

5.3 Analysis of the Closed Loop Control Elements

The above-detailed description of the closed-loop control reveals that the most relevant elements of this instantaneous process are the FIR-filters and the PLLs. Any disturbance caused by one of these elements impacts the rest of the process and consequently makes the overall compensation process work totally wrong.

5.3.1 The FIR-Filters

The Finite impulse response (FIR) filter is well known for its stability. For such a filter the impulse response that is considered as the response to any finite length input signal, has a finite time. As an example, applied to an impulse that is made of only one sample of "1"

followed by many samples of “0”, the FIR filter delivers zeroes after the “1” sample will have made all his way through the filter. This is in direct contrast to the infinite impulse response (IIR) filter, which continues to respond indefinitely due to its internal feedback.

The simplest way to realise a FIR filter is the direct form, which is depicted in Figure 5-3. The only three basic elements needed are the gain, the sum and the single sample delay. The output value is the weighted sum of the most recent input values. The mathematical expression, also known as discrete convolution, is as follows:

$$y[n] = \sum_{i=0}^{N} b_i \cdot x[n-i] \qquad (5\text{-}1)$$

Where $x[n]$ is the input signal, $y[n]$ is the output signal, N is the FIR filter order and b_i the value of the impulse response at the i[th] discrete time. In the case of the direct form (Figure 5-3), the sequence of b_i is the coefficient list that characterizes the filter.

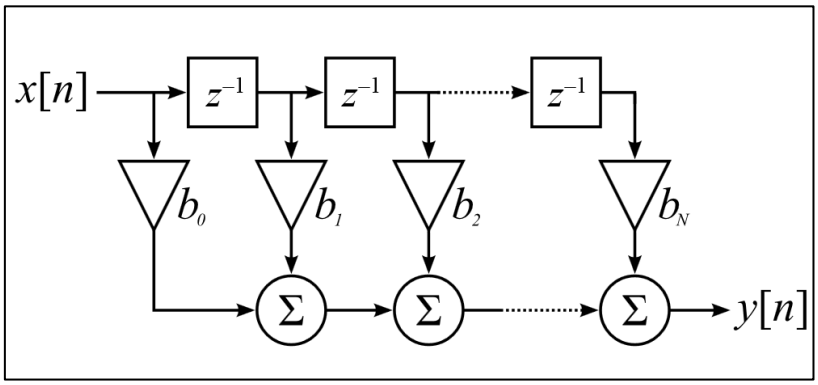


Figure 5-3: Basics of a FIR filter

Many intrinsic characteristics of an FIR filter can be deduced knowing the number N of its coefficients and their values b_i.

- The impulse response is set by the coefficients: This can be understood as the output value of the filter if a one sample impulse of value “1” followed by “0” samples are put in the filter.
- The number of filter taps: A tap is a pair of one coefficient and one sample delay element. It is equivalent to the number of coefficients N. This gives a good indication of the amount of memory required by the filter and the number of calculations. It is also representative of the filtering efficiency because more taps means a better stopband attenuation, a narrower transition band and less ripple.
- The time delay T_d: It is actually quite simple to determine the time delay of the FIR filter. It depends only on the taps number N and the sampling frequency f_s.
- $T_d = \frac{N-1}{2 \cdot f_s}$
- For example, a 101 taps linear-phase FIR filter operating at a rate of 10 kHz has a delay of 5ms. Another filter having 401 taps with a sampling frequency of 20 kHz will have a 10ms time delay. This is very interesting for periodical input signal like AC voltages. The time delay can immediately be interpreted as a phase-shift. For a 50Hz signal, this means it has a period of 20ms, 5ms is the quarter of it period this means a phase-shift of 90° and similarly, 10ms time delay corresponds to a 180° phase-shift.

In order to illustrate the impact of the number of taps of the FIR filter, two band-pass FIR filters have been designed. They both have the same 20 kHz sampling frequency, the same windowing type and also the same passband width of (250±10%) Hz but one has 401 coefficients while the second has 201. Figure 5-4 shows the frequency response of the two designed filters in function of the normalized frequency. They both have 0 dB attenuation at the rated 250 Hz frequency but the filter with greater coefficients number depicts a better attenuation for the surrounding frequencies this means a narrower transition band. The filters phases are also influenced by the number of taps. The 401 taps filter has a phase of -180° while the 201 taps filter shows a - 90° phase.

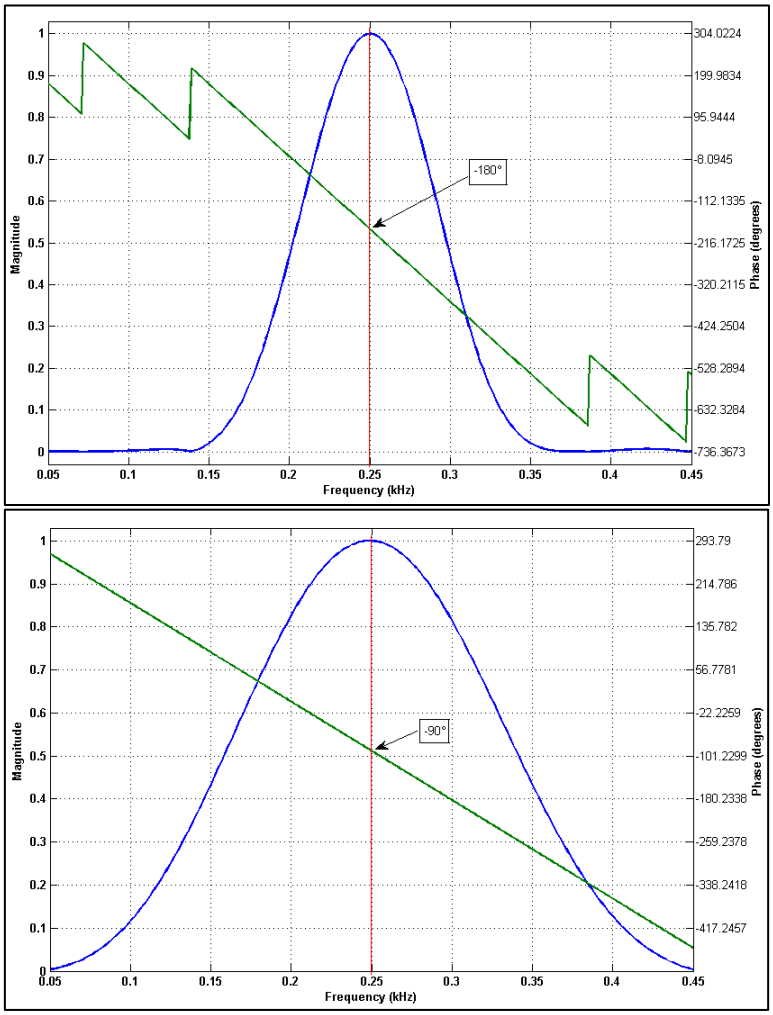


Figure 5-4: Passband Comparison of Two FIR Filters with Different Number of Taps: 401 (top) and 201 (bottom)

Regarding the filter phase of the band-pass FIR filters, the time delay of the filter (depending on the number of taps and the sampling frequency) is the key factor. The MATLAB tool for filter designing Filter Design and Analysis Tool (fdatool) is used to generate some empirical values that reflect the relationship between the filter time delay, and the filter phase shift. Table 5-1 shows the computed phase shifts for different band-pass filters characteristics. The filters have the same bandwidth (the same as in the previous paragraph: bandwidth 250Hz ±10%) but a different number of taps and/or a different sampling frequency.

Table 5-1: Time Delay and Phase Shift for Three FIR Filters with Different Number of Taps

	Fs=10 kHz		Fs=20 kHz		Fs=40 kHz	
N	dt (ms)	ρ (°)	dt (ms)	ρ (°)	dt (ms)	ρ (°)
101	5	-90	2,5	-225	1,25	-112,5
201	10	-180	5	-90	2,5	-225
401	20	-360	10	-180	5	-90

These phase shifts are for a 250Hz input signal. The input signal period T_{in} is then 4ms. Taking for example the 100 taps filter with a 10 kHz sampling frequency, its time delay is 5ms. This is 1.25 times T_{in}. Since they are periodic values, integer multiples of the input signal can be neglected and the phase-shift will be only the remaining fractional multiple of the input period. This means that the filter will have a 5ms total time delay, but shows only a quarter period delay, i.e. 90°. The same reasoning can be applied for the 200 taps filter with 40 kHz sampling frequency. The time delay is 2.5ms this corresponds to 5/8 of the 250 Hz input signal period. Therefore, the final phase difference in degree is 5/8 times 360, i.e. 225°. This leads to the following fast formula.

$$\rho_{BPF}[°] = \left(\frac{N-1}{2 \cdot f_s \cdot T_{in}}\right) mod\ 1 \times (-360°) \qquad (5\text{-}2)$$

The Figure 5-5 is another illustration of the phase shift caused by the FIR filters. The output values of three filters have been compared. The input signal a 250 Hz signal sampled at the 20 kHz. Each filter has the same bandwidth as before but the first has only 100 taps, the second 200 and the third 400. The above-calculated phase shift can easily be observed on the graphs. Especially on the last plot, where the 180° phase difference appears clearly as the opposite of the input signal. The bigger the number of taps, the longer is the transient phase.

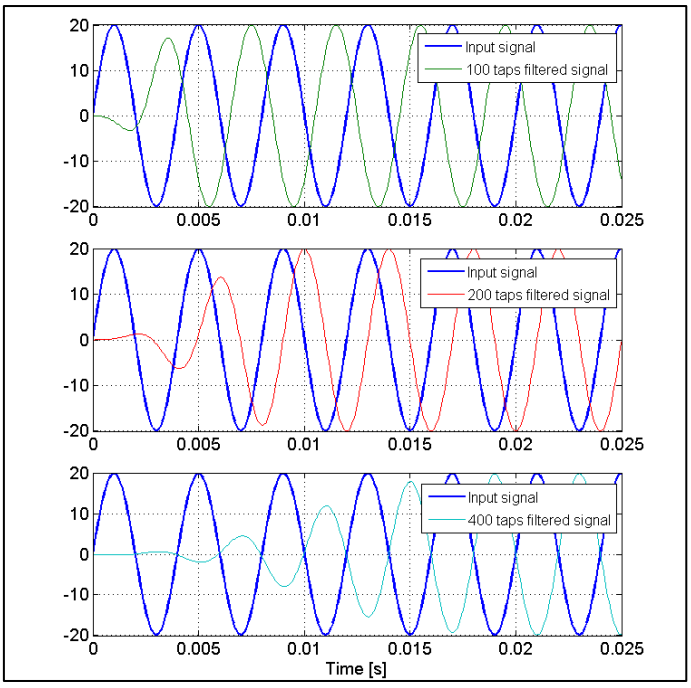


Figure 5-5: Physical Illustration of Time Delay Caused by FIR Filter Depending on the Number of Taps

On the one hand, the FIR filter, compared to the IIR filter, has the following advantages:

- It is easy to design in order to have a linear phase: this is done by using a symmetric coefficient sequence. The filter introduces a time delay but no phase shift.
- It is less complex than the IIR of the same order
- It is generally less sensitive to errors or noise due to the absence of the feedback that might cumulate the errors
- It has very convenient numeric properties: in practice, the DSP must be implemented using arithmetic with limited precision (limited number of bits). For the IIR filter, this could be a problem due to the feedback that will accumulate the rounding errors. Since this problem does not exist for the FIR filter, it can be designed with a lower precision demanding thus less computational power.

On the other hand, the FIR filter is less selective than the IIR one with the same order. This means the bandgap between the passband and the stopband is bigger than that of the IIR. Generally, the FIR filter requires more memory and/or repetitive calculation.

To come back to the design of the control system, each harmonic's filter has been designed as a symmetric 400^{th} order band-pass filter with the bandwidth frequency defined as the harmonic frequency $\pm 10\%$. This has been realised in MATLAB using the Hamming window function. The sampling frequency is 20 kHz. The resulting filter characteristics for the fundamental (50 Hz), the 5^{th} harmonic (250 Hz) the 7^{th} harmonic (350 Hz) are shown in Figure 5-6. The coefficients are symmetric around the median 200^{th} value. The values of the coefficient of the harmonics filters are oscillating and the number of oscillations is equal to its rated harmonic frequency compared to the fundamental. The coefficients of the 5^{th} harmonic filter are oscillating 5 times while those of the 7^{th} are oscillating 7 times. The magnitude responses show no attenuation at the rated frequencies. This attenuation factor does not decrease rapidly around the rated frequencies so that in the wished frequency variation range, it remains more than 80% of the filtered signal. Finally, the phase shift for the fundamental filter is -180°. According to the quick formula in (5-2), all the harmonic filters will have phase shifts that are equal to the harmonic order times the fundamental filter phase (-180°). The result is a common -180° phase shift for all the harmonics FIR filters (-180°*5=-180°, -180°*7=-180°…). The reason is that the harmonics frequencies are only odd integer multiple of the fundamental frequency. This -180° common phase shift is a very good simplification tool since the output signal simply has to be multiplied by -1 to correct the phase of the filter.

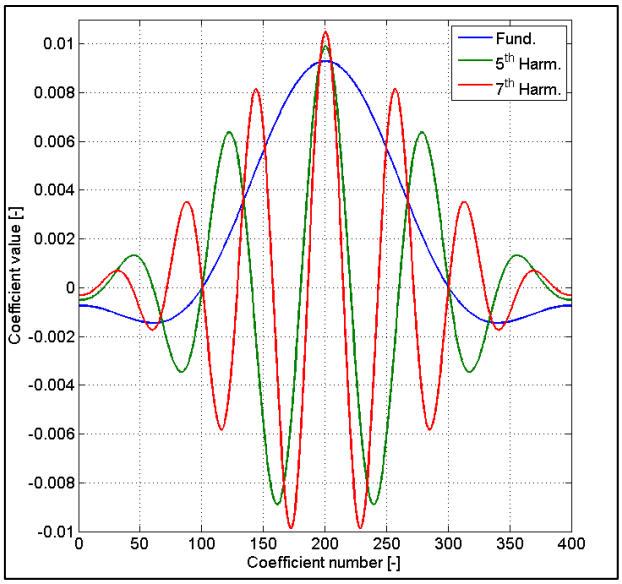


Figure 5-6: FIR Coefficients Values for 50 Hz, 250 Hz and 350 Hz Band-pass Filters with 400 taps

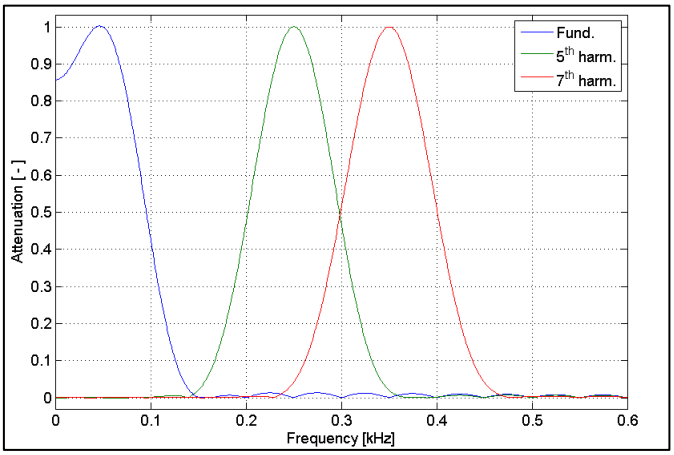


Figure 5-7: Attenuation Value of 50 Hz, 250 Hz and 350 Hz Band-pass FIR Filters with 400 taps

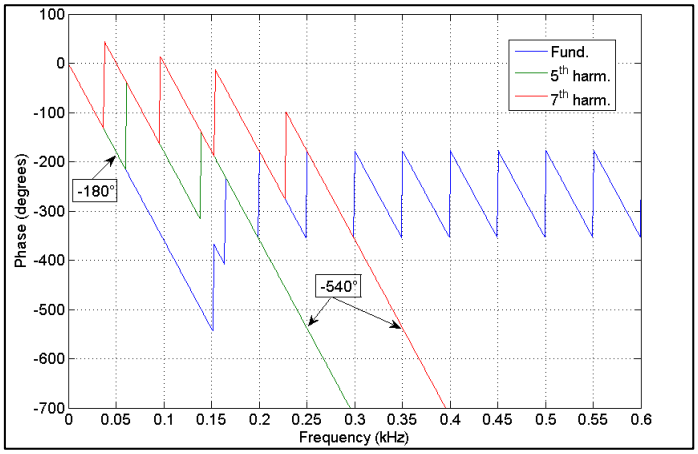


Figure 5-8: Angular Phase-shift Value for 50 Hz, 250 Hz and 350 Hz Band-pass FIR Filters with 400 taps

5.3.2 PLLs

The implemented PLLs for the harmonic compensations have all the same SRF dqPLL structure. This structure is chosen among the others because of the DC shape of the voltage components in the dq-frame in order to apply purposely the classical control methods in the controller's structures later on. Effectively these steady-state values are perfect for the regulation of the voltage magnitude through a PI controller. Each PLL feedforward angular frequency

corresponds to its dedicated harmonic frequency. This gives to the PLL system a fast convergence to the steady-state operating point that should be the synchronization to the harmonic angular velocity. (4-30) gives a good indication on how the PLL coefficients values can be chosen. The PLL of the signal at the fundamental frequency has small coefficients since the magnitude of the signal is much higher than that of the harmonics. The PLL coefficients of the harmonics signals require more attention because their magnitude does not remain constant due to the compensation, which changes the dynamic of the PLLs. Before the compensation starts, the magnitude of the harmonics is maximal. A given set of coefficients brings a certain dynamic for that maximum magnitude. However, with the same set of coefficients, during the compensation process, the magnitude of the harmonics decreases. This changes the whole PLLs dynamic by making it slower than that for higher magnitude values (with the same coefficients). Any disturbance like a slight frequency change takes then longer to be recovered. This leads to the idea of a controller with adaptive gains, where the values can be adapted to the detected harmonics magnitude to ensure a constant PLL response time. Since the maximum harmonic magnitude can easily be approximated (a percentage of the fundamental amplitude inversely proportional to the harmonic order), a good compromise can also be found by fixing the values of the coefficients appropriate for the half of the estimated maximum amplitude. With this solution, the PLL would not be so fast at the beginning but also not so slow, once the harmonic amplitude will reach its minimum due to the compensation.

In order to illustrate this behaviour, the following scenarios have been simulated in Simulink. The phase angle of a constant 100V 50Hz signal is detected with a dqPLL with $\mathrm{k_p} = 4\ \mathrm{rad}V^{-1}\mathrm{s}^{-1}$ and $\mathrm{k_i} = 25\ \mathrm{rad}V^{-1}\mathrm{s}^{-2}$ (scenario 1). After a half second, the frequency of the input signal is increased by 2%. The second scenario (scenario 2) is simulating a harmonic compensation process. The same initially 100V and 50Hz input signal sees its magnitude constantly decreasing from the time 0.1 sec to reach 20V at the time 0.5 sec (time of the frequency change) till a stationary value of 5. The Figure 5-9 shows the comparison of the delivered detected phase angle by the PLLs. First, it can be observed that the magnitude decrease in the scenario 2 does not affect the PLLs output phase angle. The two PLLs delivered the same phase angle even if the amplitude of the input signal of the second PLL is decreasing. The previously described dynamic change in function of the magnitude can be observed after the frequency change. On the one hand, the first PLL working with the unchanged magnitude recovers to the correct phase angle in less than 100ms. On the other hand, the PLL dealing with the signal with decreasing magnitude (only 20 at 0.5 sec) presents a long oscillatory correction that needs much longer (1000ms) to find the stabilized correct phase angle. Furthermore, the peak error of the phase angle is four times higher for the second scenario than for the first one. This could be a big disadvantage for very sensitive and phase angle dependent control systems. Practically this does not have a big impact on the stability of the harmonics control of an APF, since the maximum error of the phase angle is not large enough to change the compensatory effect of the generated harmonic voltages. The sum of two sine waves of same magnitude but with a phase angle different of $\pm\frac{2\pi}{3}$ will result in another sine wave with the same magnitude. The resulting magnitude is higher or lower if the phase shift is respectively lower or higher than that limit. This reminds us the three-phase voltages system. Accordingly, for the harmonic compensation, a phase error of up to 60° will still lead

to a reduction of the remaining harmonic. Furthermore, the harmonic magnitude control will gradually improve its harmonic compensation since the PLL will progressively reduce the phase error.

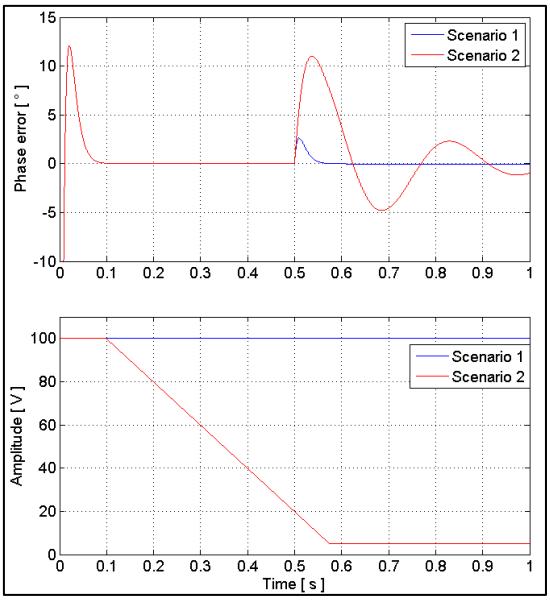


Figure 5-9: PLLs Dynamic Comparison in Function of the Input Signal Magnitude

5.3.3 Harmonics Magnitude Controller and Harmonic Compensation Signal Generation

The magnitude of the harmonic is controlled by regular PI controllers. The controlled values are the DC dq-frame harmonic voltages components u_d and u_q delivered by the PLLs. This means also that 2 controllers are required for the magnitude control of one single harmonic voltage and the output values of the controllers represents the compensatory value for u_d and u_q. These values are transformed back into the 3-phases system through the inverse Park and inverse Clarke transforms using the instantaneous phase angle delivered by the PLL. The dynamic of the controller, determined by its coefficients $\mathrm{k_{pCtrl}}$ and $\mathrm{k_{iCtrl}}$ is critical. A slow controller needs longer to compensate the harmonic completely, while a too dynamic one might bring some instability issues. A simple numerical compensation model has been realised in Simulink (Figure 5-10) to show how the compensators (harmonics voltage controllers - Figure 5-11) can affect the whole system.

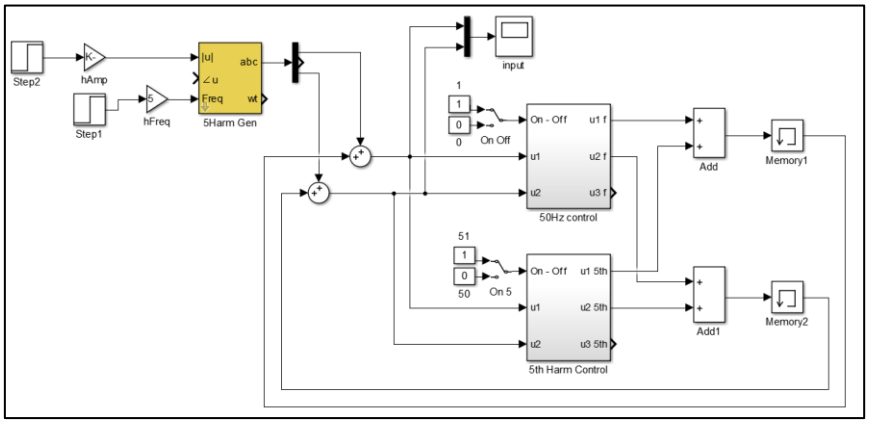


Figure 5-10: Simulink – Basic Numerical 5th Harmonic Compensation on a 50 Hz Generated Signal

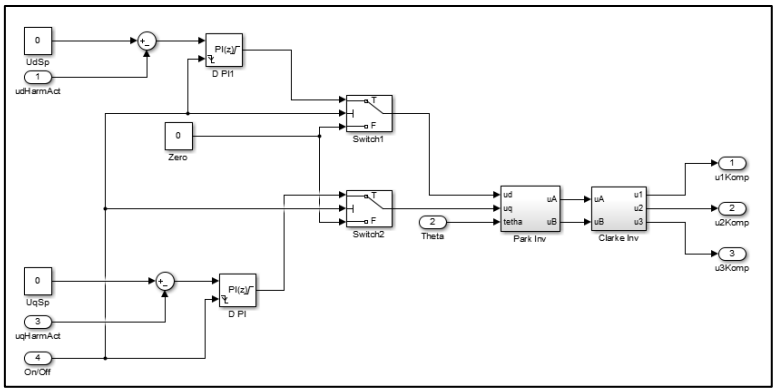


Figure 5-11: Harmonic Magnitude Control and Compensation Voltages Generation

The 50Hz control has to generate and control a 400V RMS fundamental frequency. At the same time, a 250Hz harmonic distortion with a magnitude of 40V is created and added to the fundamental value. The investigated 5^{th} harmonic control has to detect the distortion caused only by the injected 5^{th} harmonic and compensate it so that the final input signal is harmonic free. In this case, the system (electrical components) is supposed to have a proportional transfer function equal to one. The compensation starts at the time 0.2 sec.

Some simulation results are shown in Figure 5-12 and Figure 5-13. The blue plot is the existing, i.e. remaining harmonic to be eliminated and the red plot is the injected correcting harmonic. They show that the system remains stable and compensates very good with only an integrator gain k_i. The value of $k_i$impacts the rapidity at which the harmonic is completely compensated. The perfect configuration of the controller coefficients is strongly dependent on the transfer function from the controller output to the harmonic source. Delays and attenuation factor are very critical. In the discussed example, the output of the controller has a direct and full impact on the harmonic, but this is not the case in real conditions. Since there are no constraints on the speed of the harmonic mitigation, it is better to trade off the stability rather than the speed. Controllers with low dynamics will still be able to mitigate the harmonics even if it takes 10 seconds more than the more dynamic ones.

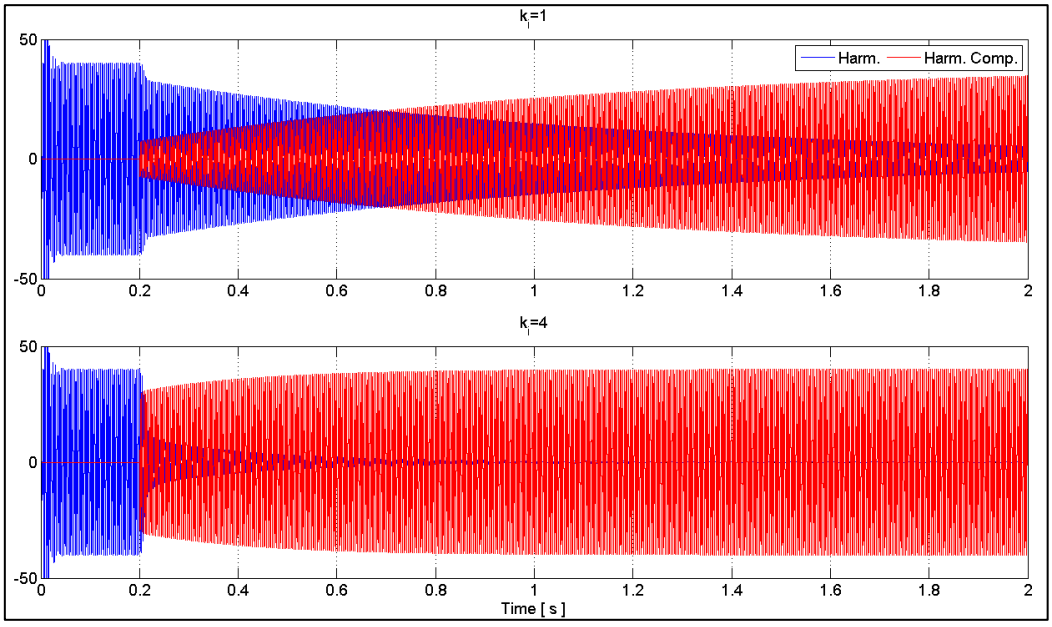


Figure 5-12: Harmonic Compensation with Only an Integrator Controller

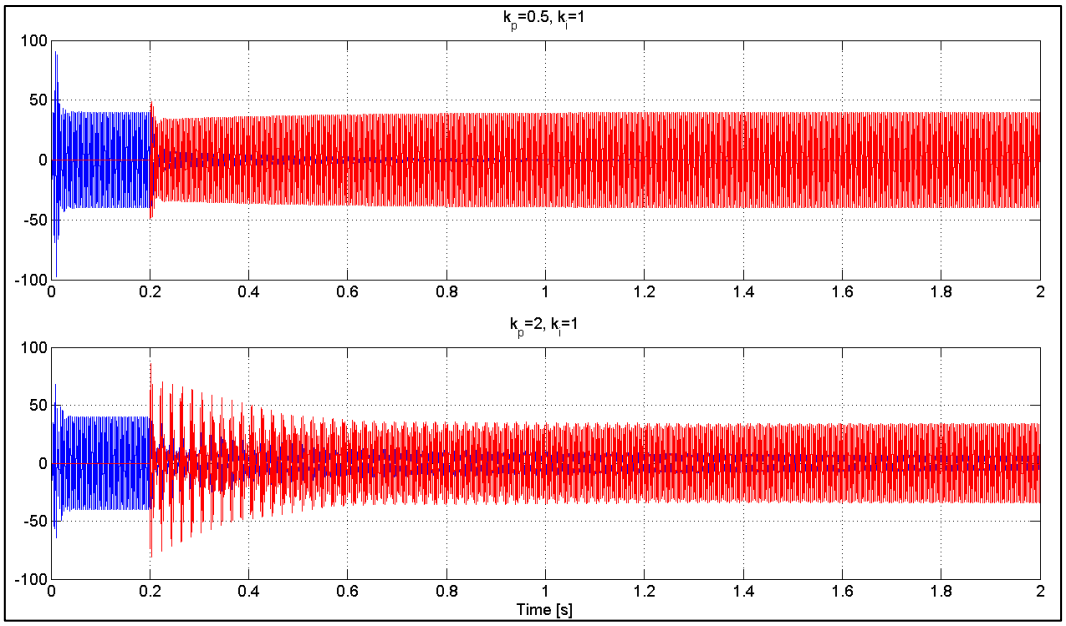


Figure 5-13: Harmonic Compensation with a PI Controller

5.3.4 The PWM Voltage Generation

The PWM represents the key element when it comes to transforming a DC voltage into an AC voltage. A simplified transfer function can be summarized as the efficiency, at which the PWM manages to generate a given sinusoidal wave. In order to estimate this proportional transfer function coefficient, a comparison will be done between a reference sinusoidal input signal used for the PWM generation and the output PWM voltage. Since the PWM output voltage is made out of fast impulses, an FFT will extract only the percentage of the input signal that is contained in the output signal.

5.3.4.1 Intersection Modulation

This method represents the simplest PWM generation method. The reference sinusoidal signal is compared to a high-frequency carrier signal that can be a sawtooth or a triangle. When the value of the reference signal is higher than that of the carrier, the switch is turned on, otherwise, it is turned off. The performed simulation is described as follows: a 50 Hz reference sine wave with a magnitude of 100, along with a 15 kHz triangle carrier signal are used to generate PWM firing signals for a 400V DC fed inverter. The triangle signal has the same amplitude as the amplitude of the DC voltage. The PWM voltage output by the inverter is analysed with the Fourier method to get the amplitude and the phase of the 50 Hz component present in the high-frequency PWM. The results depicted in Figure 5-14 show that the 50 Hz voltage is a little bit attenuated since the output amplitude is lower than expected notably 87V instead of 100V. Further simulations have shown that modifying the modulation index by changing the value of the DC branch that is also the triangle amplitude, or the amplitude of the reference signal does not have any impact on the attenuation factor. The carrier signal frequency has also been varied but it presents no major impact on the amplitude reduction degree. The attenuation factor a_{SinTr} for the PWM generated by the intersection method for a 50 Hz reference signal is then

$$a_{SinTr} = \frac{(100 - 87)}{100} = 13\% \qquad (5\text{-}3)$$

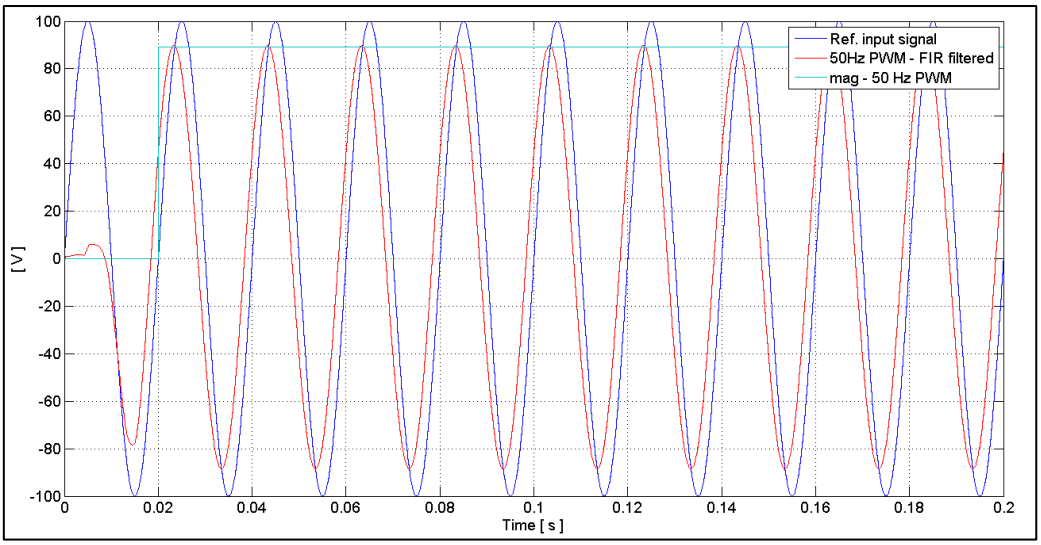


Figure 5-14: Input Signal and Output Voltage of an Inverter Controlled by the Intersection Method

The same result is obtained when the reference signal frequency is changed (test done for the 5th, 7th, 11th, 13th and 17th harmonics of a 50 Hz reference signal). It can be concluded that for any reference signal frequency and amplitude, the intersection method will transfer only 87% of the reference signal magnitude assuming that the voltage drop of the inverter IGBTs is negligible. This makes it easy to correct this attenuation in order to have a 100% transfer of magnitude between the output signal and the input reference signal. The correction can be done either by reducing the triangle amplitude by the attenuation factor, or by increasing the reference signal as the signal is multiplied by the inverse of the transfer gain ($1-a_{SinTr}$). The Figure 5-15 compares the obtained magnitudes for a normal intersection PWM and a corrected one. The corrected magnitude of the PWM output matches that of the reference input signal. The phase shift appearing after the triangle magnitude correction decreases slightly (from -30° to -27°).

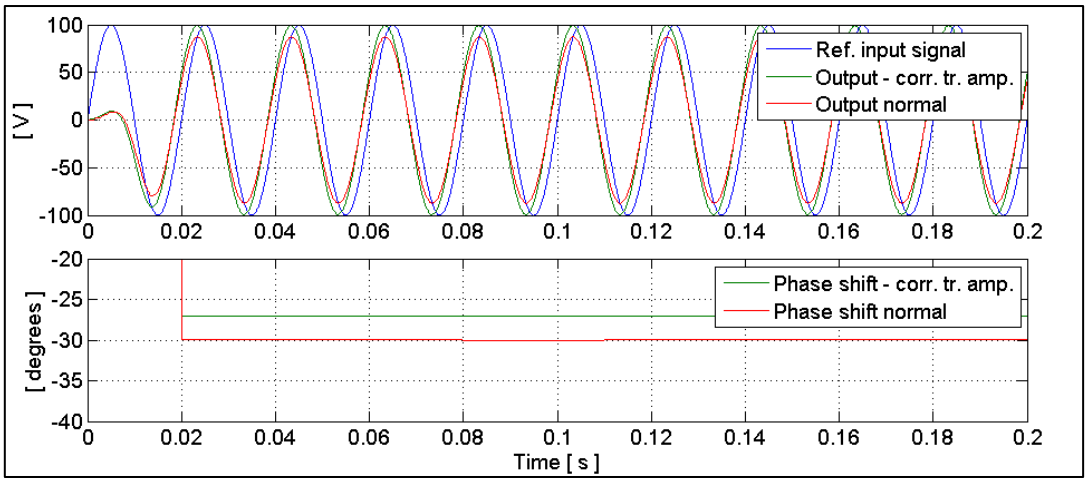


Figure 5-15: Output Voltage and Phase-shift after Correction of the Triangle Wave Amplitude

Concerning the voltage phase shift due to the PWM, analyses have been realised, where the input and the output phases of the signal are compared at different frequencies. A constant phase difference of approximately -30° is noticed for the non-correction intersection method and this value decreases by 2 to 3° when the carrier triangle magnitude is adjusted (reduced by the attenuation factor). This remains constant independently of the reference signal or the carrier signal frequency.

5.3.4.2 Space Vector Modulation

Unlike the intersection method that can easily be implemented in analogue circuits, the space vector modulation is a little bit more complex algorithm. The sinusoidal reference signal is transformed into its corresponding rotating vector (polar coordinates) and depending on its position (angle) and amplitude compared to the maximum amplitude; the switching times between different predefined states are calculated. The different states are defined so that a short circuit of the DC voltage source never happens. The transfer function check is similar to the tests done for the intersection method. According to the results depicted in Figure 5-16 for a PWM frequency of 9.9k kHz, the space vector modulation (SVM) generates a PWM which nearly contents 100% of the reference signal. The Fourier calculated amplitude is 102.25 for a 100V amplitude reference signal. The phase shift is also different from that of the intersection method and is nearing 120°. These values remain sensibly constant by different PWM frequencies. (103V and 116.7° for a 15 kHz PWM; 102.1 V and 118.8° for the 6 kHz PWM).

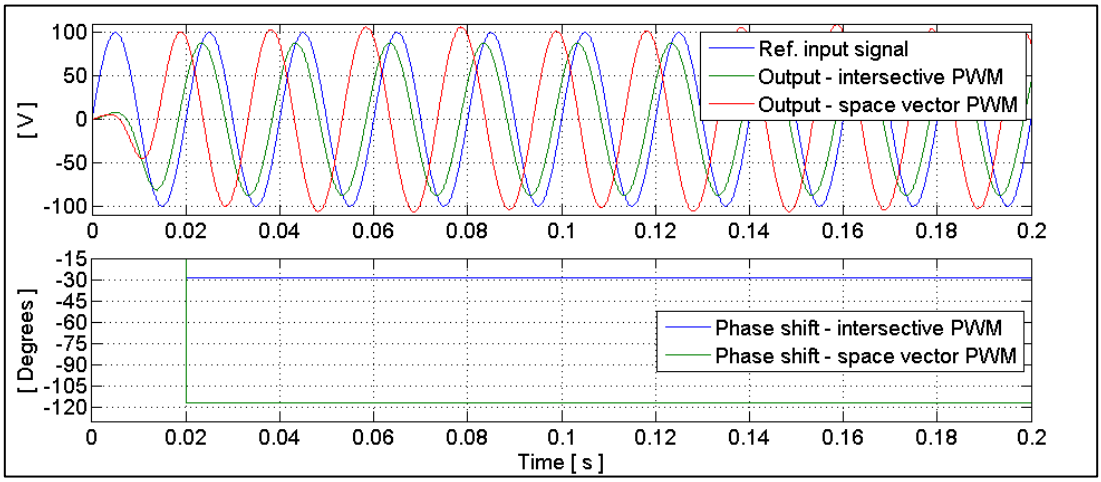


Figure 5-16: Space Vector and Intersection PWM Output vs Input Signal

Despite the almost perfect signal transfer of the SVM, the amplitude transfer efficiency varies with the modulation index, which is the ratio of the magnitude of the reference signal to the magnitude of the maximum output (DC voltage) but the variations remain very small especially in the cases, where the modulation index is more than 50%.

Table 5-2: Relative Efficiency and Phase-shift of the Space Vector PWM for Various Modulation Indices Values

DC mag. [V]	Ref. sign. Mag. [V]	Mod. Index [-]	Output mag. [V]	Efficiency [%]	Phase shift [degrees]
400	50	1/8	53,7	107.4	117.5
400	100	1/4	102.4	102.4	118.35
400	150	3/8	150.7	100.47	118.5
400	200	1/2	201.3	100.65	119
400	250	5/8	249.8	99.92	119
400	300	3/4	298.6	99.53	119.05
400	350	7/8	348.6	99.6	119.2
600	500	5/6	498.5	99.7	119.2

5.3.4.3 Conclusion

The two PWM methods manage well the transfer of the given reference signal. The intersection method needs to be adjusted, due to the attenuation (13%) in order to have a 100% amplitude transfer coefficient between the output and the input reference signal. Both

methods induce a phase shift that can be approximated to 30° and 120° for the intersection and the SVM methods respectively. On a modelling point of view, they can be considered as a voltage phase shifter. The SVM is the most popular PWM technic despite the more complex generation of the switching signals. The main benefits of the SVM are a higher DC branch utilization, lower energetic switching losses, a better harmonic spectrum (lower THD) [90] [91] on the one hand. On the order hand, the intersection PWM is very cheap because it needs simple components and can also be realised with analogue components.

5.4 The Power Inverter as an Auto-compensated Voltage Source

The compensation structure described in the previous chapter is now going to be tested in a real electrical circuit. The disturbing harmonics are no longer mathematically generated but will come from a real nonlinear load. The power source is made of a battery fed VSI followed by a passive low-pass filter used to cut-off the high frequencies voltages above 1 kHz contained in the VSI PWM voltage output. The VSI is controlled based on the sinus-triangle method where a high-frequency triangle signal is compared to the sinusoidal voltage signal to be generated. The non-linear load is made of a resistive load connected to the power source through a passive 6-diodes rectifier. The compensation system measures the level of the different harmonics generated by the non-linear load, and then generates a distorted voltage source so that the harmonic distortion generated compensates the existing harmonic distortion. As a result, the apparent voltage at the PCC is harmonic free. This process is first tested in a simulation MATLAB Simulink and then on a test bench in the lab.

5.4.1 Simulated Compensation by the APF

For the simulation, the electrical LPF is modelled as a parallel RLC filter as shown in Figure 5-17.

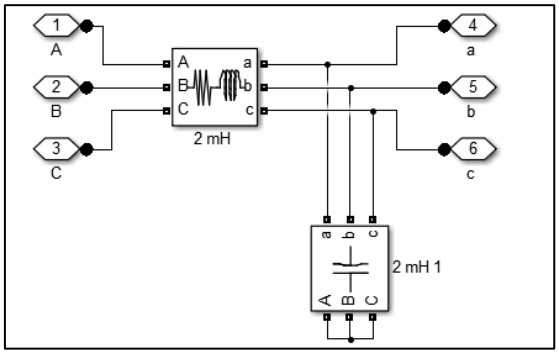


Figure 5-17: Low-pass RLC Filter Topology

The filter parameters are $R = 1\Omega$, $\mathrm{L} = 1.58\mathrm{mH}$ and $\mathrm{C} = 70\mu\mathrm{F}$. The load is a 10kW resistance connected at the filter output through a 6-diodes bridge (Figure 5-18).

The compensation of each harmonic starts one after the other with 0.3 sec delay from the lowest order (5^{th}) to the highest (17^{th}). The non-linear load is connected at the time 0.15 sec and the first compensation (5^{th} harmonic) starts at the time 0.5 sec. The following figures show the compensation results.

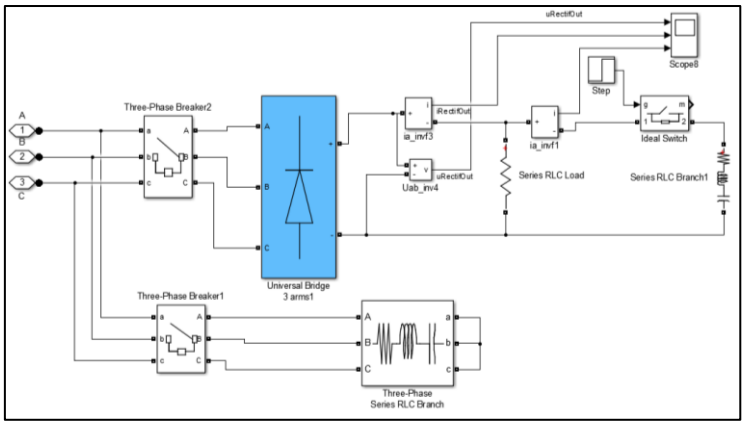


Figure 5-18: Parallel Loads Including a Bridge Rectifier Fed Load

In order to get results that would best reflect the reality, the model of the LPF is modified. According to the installed filter on the test rig, the filter topology is shown in Figure 5-19 and has the following characteristics: the capacitances, $7\mu F$ each, are connected in star. Each inductance has a value of $1.58mH$ with a resistance of $0.2\ \Omega$.

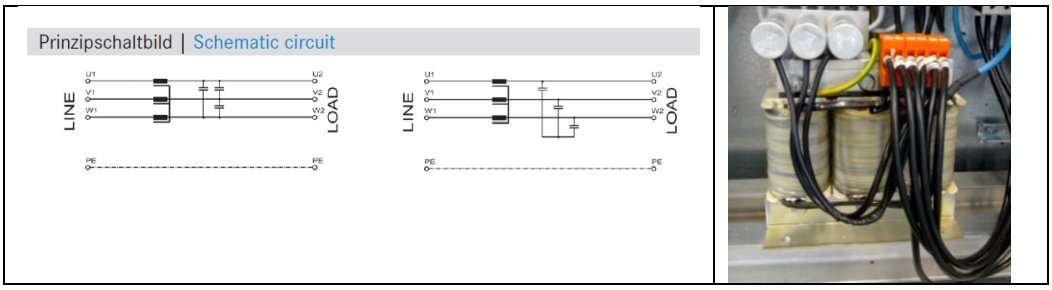


Figure 5-19: Schematic Circuit and Picture of the LC Filter on the Test Rig

5.4.2 Passive Low-pass Filter Modelling

The low-pass filter connected to the output of the VSI should remove the high frequencies from the PWM voltage generated (by the VSI). On the data board on the LPF in the lab (Figure 5-19), it is indicated that the minimum switching frequency of the inverter is 4 kHz (16 kHz max), the inductance and the capacitance are 1.58mH and 7µF respectively. However, there is no information concerning the windings and the ferromagnetic core. The datasheet of the filter indicates a 165W power loss at nominal working point (400V and 40A) and a 4 to 5% voltage drop.

The filter can be modelled as an RLC circuit where the inductance L with an internal resistance R is connected in parallel with the capacitance C as depicted in Figure 5-20.

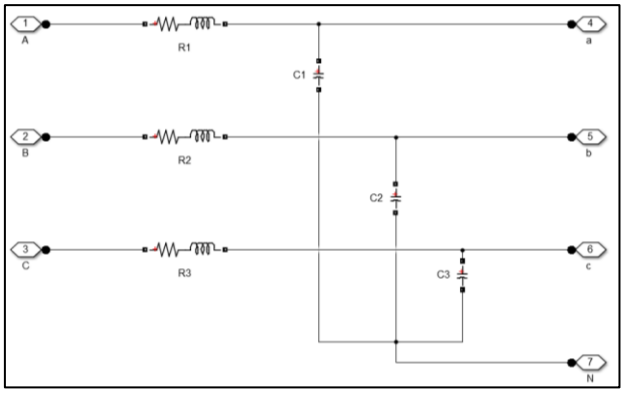


Figure 5-20: RLC Branch as Low Pass Filter

A simulation of the filter as an RLC branch depicts good results as shown in the following figures. The PWM is generated based on a 15 kHz triangle wave. The inverter is fed by a 600V DC voltage source. The inverter reference sine wave has a frequency of 50 Hz and a phase RMS magnitude of 220V. The filter inductance and capacitance have the values indicated by the manufacturer and the resistance is set to the measured value 0.2Ω. Figure 5-21 shows the output voltage characteristics first by no load then after pure resistive load drawing the maximum current of 40A is connected. The filter has a very good efficiency since the output voltage has a THD of about 6% dropping to about 4% when the current reaches its maximum value in a linear load. Another critical point is the voltage drop after connecting the load. The RMS values decrease from 220.5V to 210.5V. This corresponds to a 4.54% voltage drop and then matches the indicated 4 to 5% voltage drop range indicated by the constructor.

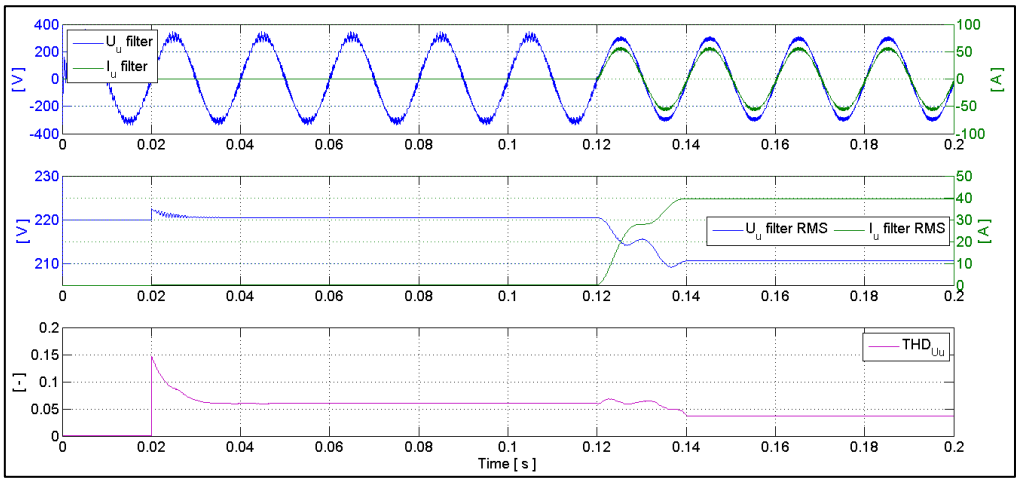


Figure 5-21: Output Voltage of the Passive RLC Filter with Linear Load

Further investigations have shown that using a PWM frequency lower than the indicated minimum frequency of 4 kHz causes the output voltage to have a THD higher than the accepted standard value (8%). This corroborates with the FFT analysis depicted in Figure 5-22 that shows the magnitude content of the filter output voltage obtained for different PWM frequency. The lowest switching frequency depicts the highest content of high frequencies especially around 1500 and 3000 Hz. The 15 kHz switching frequency displays the least content in high frequencies.

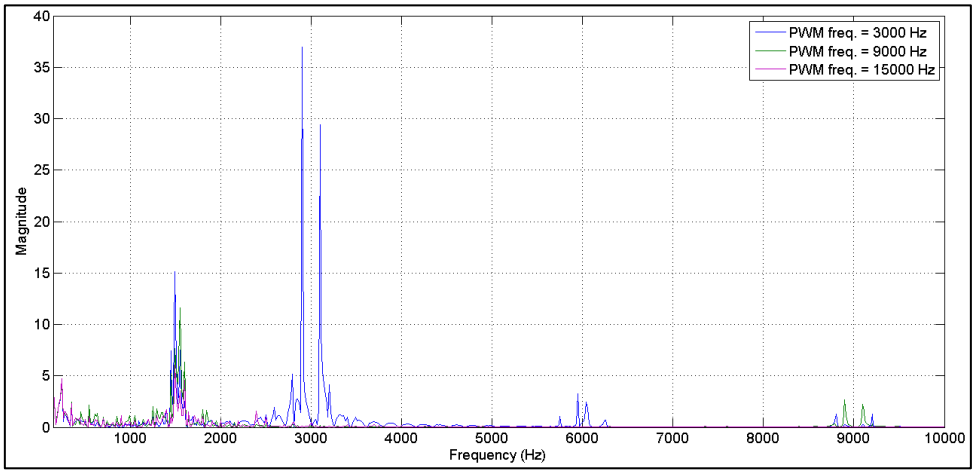


Figure 5-22: Magnitude Spectrum of the Filter Output Voltage vs PWM Frequency

In the case of a non-linear load, modelled as a diode bridge rectifier feeding a resistance at nominal power, the computed voltage drops by 3.95% while the THD of the output voltage, as expected, increases from 6 to 20% (Figure 5-23).

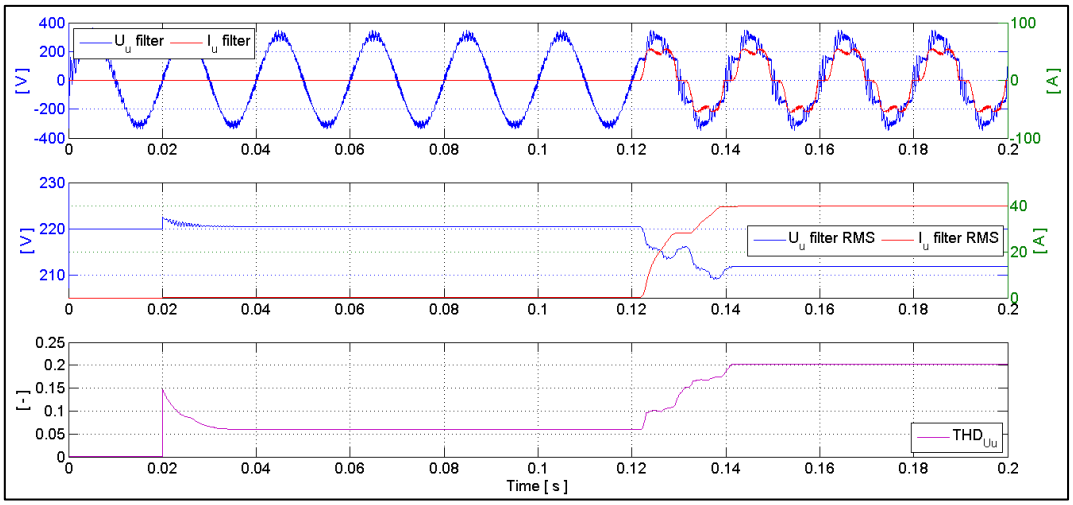


Figure 5-23: Output Voltage of the Passive RLC Filter with a Non-linear Load

5.4.3 Simulation Results

The whole compensation system has been set up for a simulation in MATLAB Simulink. The control system is running at a sampling frequency of 20 kHz for a simulation duration of 2 seconds. The triangular signal used for the PWM control has a frequency of 20 kHz. The band-pass FIR filters, as well as all the PLLs, have a sampling frequency of 20 kHz. The PI controllers-duo of the magnitude (u_d and u_q controller) for each frequency are setup as indicated in the following Table 5-3. They all have the same sampling frequency set at 20 kHz.

Table 5-3: Configuration of the Fundamental and Harmonics Magnitude Controllers

	K_p	K_i	Control starting time (s)		K_p	K_i	Control start (s)
Fund. Freq. (50 Hz)	0.1	20	0.0	11th harmonic	0.1	8	1.1
5th harmonic	0.1	8	0.5	13th harmonic	0.1	8	1.4
7th harmonic	0.1	8	0.8	17th harmonic	0.1	8	1.7

As a first positive result, the fundamental identification and control methodology works properly as expected. The magnitude of the fundamental voltage converges and stabilises at the 560V magnitude set point. When the load is connected at the time 0.15 s, the 50Hz voltage amplitude is not in its steady state condition yet but its magnitude controller corrects the voltage drop, adjusts and finally reaches the final value after about 200ms. After the non-linear load is connected, the magnitudes of all the harmonics increase. This transitory phase shows a variation of the harmonic magnitudes, but the steady state of the harmonic detection is reached 250ms after the load connection. Once a particular harmonic compensation starts, it can be noticed that its magnitude is decreasing to a final value very close to zero. A very interesting point here is to observe the interaction between the harmonics. The reduction (compensation) of the 5th harmonic influences the magnitude of the other harmonics. The magnitude of the 7th harmonic increases as well as that of the 13th harmonic but the magnitudes of the 11th and the 17th harmonic decrease. Once the compensation of the 7th harmonic starts in addition to the previous compensation of the 5th harmonic, the contrary impact appears on the higher frequency harmonics, that means the magnitudes of the 11th

and 17th harmonics increase while the magnitude of the 13th harmonic decreases. Adding the compensation of the 11th harmonics causes an increase of the 13th but a decrease of the 17th harmonic but this last increases when the 13th harmonic decreases due to its additional compensation.

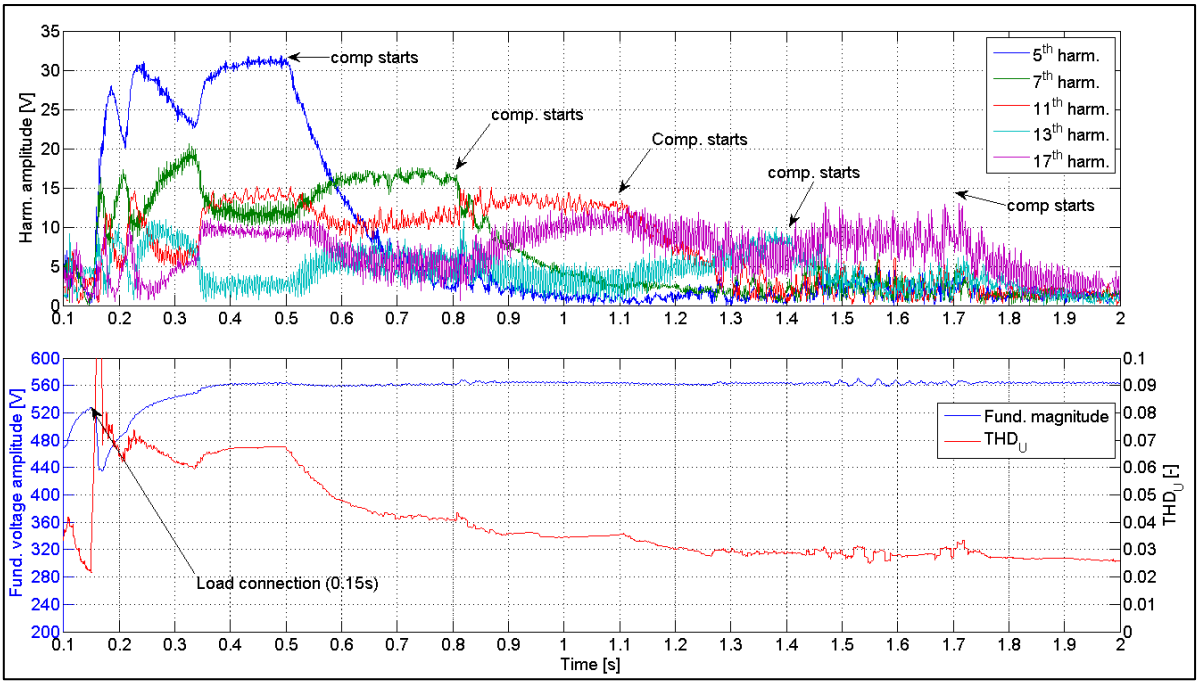


Figure 5-24: Compensated Harmonics Magnitude, Fundamental Voltage RMS Value and THD

The interaction between the harmonics compensators previously described is only about the impact of the compensation of the compensation of a low harmonics frequency on the immediate higher one. The Table 5-4 summarises the observed interaction where + means an increase and – a decrease of the harmonic magnitude. The value C indicates that harmonics is compensated. Therefore, the column of cumulated compensated harmonics means that from the left to the right, the compensation of one harmonic is realised in addition to that of the other harmonics before (lower frequencies). It can be noticed that, for this particular type of load, a simultaneous compensation of the harmonics until a given frequency automatically leads to an increase of the next harmonic order.

Table 5-4: Impact of Cumulative Compensation of Consecutive Harmonics on Harmonics of the Next Orders

	Cumulated compensated harmonics				
Impacted harmonics		5th	7th	11th	13th
	5th	C	C	C	C
	7th	+	C	C	C
	11th	-	+	C	C
	13th	+	-	+	C
	17th	-	+	-	+

Further simulation tests have been run in order to investigate if the compensation of the harmonics with high frequencies also has an impact on those with frequencies lower than the compensated one (Table 5-5). The tests were realised where only a single harmonic is compensated, and the impact on the magnitudes of the other harmonics was observed. The NA value means that the impact was not noticeable.

Table 5-5: Impact of Individual Harmonic Compensation on the Other Harmonics

	individual harmonics variation					
Impacted harmonics		5^{th}	7^{th}	11^{th}	13^{th}	17^{th}
	5^{th}	C	NA	-	-	-
	7^{th}	+	C	+	+	+
	11^{th}	-	-	C	-	-
	13^{th}	+	+	+	C	+
	17^{th}	-	-	-	-	C

These interactions could be attributed to the non-perfect harmonic compensation signals that are generated but the Figure 5-25 shows that this assumption is wrong. It shows the frequency analysis of the injected compensating signal for each harmonic. It can be seen that each compensating signal generated and injected contains only the frequency of the harmonic to eliminate. This means that the harmonic magnitude interaction noticed before is therefore related to the response of the non-linear load when the initial supply voltage is no longer a pure sine wave but a distorted sinusoidal voltage.

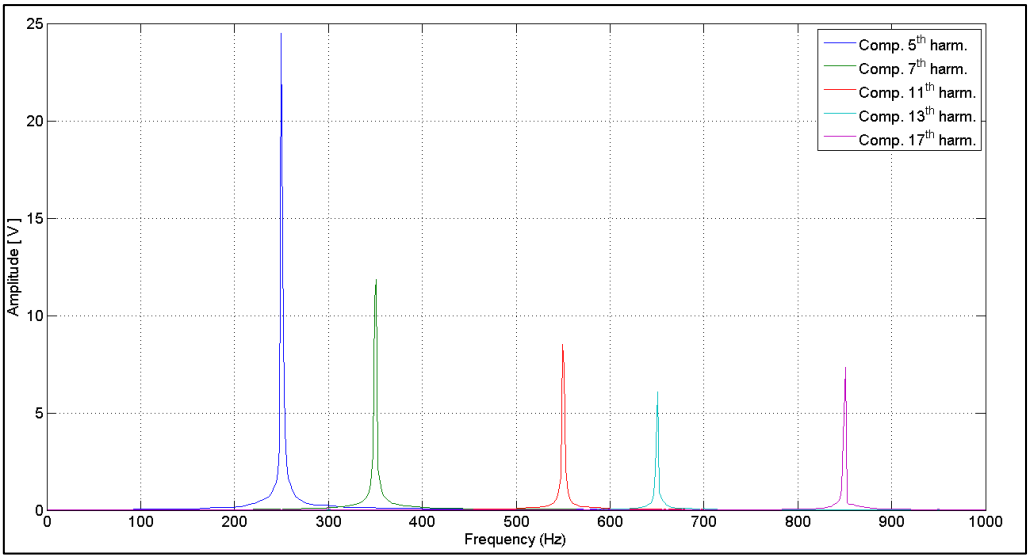


Figure 5-25: FFT Analysis of Individual Harmonic Compensating Voltages

5.4.4 Conclusion

The simulations have shown that the new compensation methodology works properly in the case of an auto compensated voltage source based on a VSI. The separated control of the fundamental frequency, as well as those of the harmonics magnitudes, works as expected. Fundamentally, the dynamic of each compensation is independent of each other. However, the results have shown that due to the non-linear response to the distorted supply voltage of the non-linear load, reducing one harmonic (by distorting the input voltage with the inverse of the existing harmonic) has an impact on the magnitudes of the other harmonics generated by the non-linear load. For the particular load studied here (6-pulses rectifier-fed resistive load), compensating the 5^{th} harmonic alternatively, increases and decreases the magnitude of the following harmonic of the higher order. An additional compensation of the 7^{th} harmonic acts on the 11th harmonic and inversely on the 13^{th} as even cancelling the magnitude reduction or increases itself due to the 5^{th} harmonic compensation. This interaction exists even though each compensation signal contains only the frequency of its dedicated harmonic to compensate.

However, the most sensitive point is the behaviour of the low-pass filter used to eliminate the high frequencies of the PWM and to transform it into a sinusoidal wave. The filter might work perfectly for the generation of the fundamental signal but depending on the filter model, the harmonic compensation could not work properly and even make the whole system unstable.

5.5 Power Inverter in Grid-tied Operations

5.5.1 Coupling of two voltage sources

Synchronising two separated voltage sources is relatively simple to achieve. Each voltage is measured separately and the controlled voltage source has to be made identical to the already existing voltage source and this in phase angle (frequency) and magnitude. Once synchronized, the coupling occurs. The connection point between the two voltage sources is called the point of common coupling (PCC) and is the closest measurement point to the second voltage source. This means that the two voltages, previously separated sources now become a single voltage source. The challenge now is to ensure the synchronism state in order to avoid unwanted power exchange between the sources. The two measurement points used for the synchronisation can no longer be considered as a tracking point. And this is so neither for the controlled source nor for the grid. Only the measured exchanged power indicates any state change like a load connection or disconnection that can induce a voltage drop or overvoltage as well as an increase or decrease of frequency. The following few lines show how the voltage at the PCC is affected by the voltage difference between both sources.

5.5.1.1 System Topology

Let us consider as one source S_i a fully controlled VSI, whose output pulse width modulated voltage is filtered with an LC filter. The second source is the power grid S_g. The inverter is synchronized with the grid and coupled at the PCC as depicted on Figure 5-26.

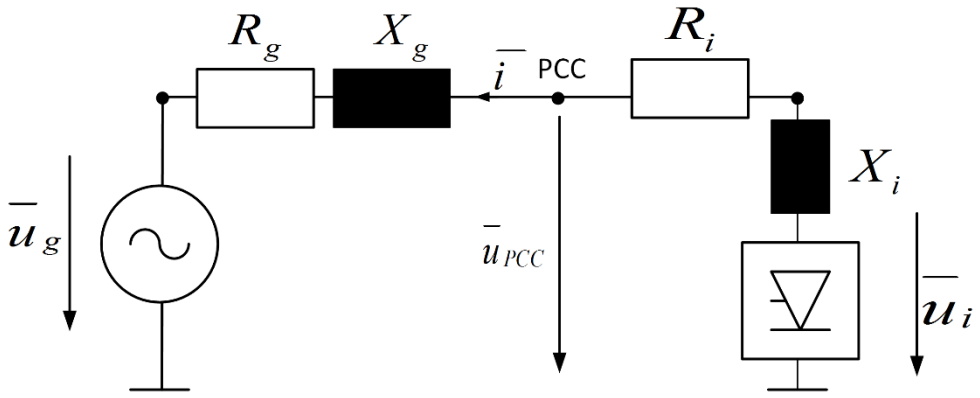


Figure 5-26: Electrical Model of a Power Inverter Coupled to a Power Grid with its Impedance

Ideally, if both sources remain stable, there would be no power flowing from one source to another since both have the same potential.

The current supplied by the inverter to the grid is

$$\bar{\imath} = \frac{\bar{U}_i - \bar{U}_g}{\bar{Z}_i + \bar{Z}_g} \tag{5-4}$$

$$\bar{U}_{pcc} = \bar{U}_i - \bar{Z}_i\bar{\imath} = \bar{U}_i - \bar{Z}_i\left(\frac{\bar{U}_g - \bar{U}_i}{\bar{Z}_i + \bar{Z}_g}\right) = \bar{U}_i\left(1 - \frac{\bar{Z}_i}{\bar{Z}_i + \bar{Z}_g}\right) + \frac{\bar{Z}_i}{\bar{Z}_i + \bar{Z}_g}\bar{U}_g$$

$$\bar{U}_{pcc} = \frac{\bar{Z}_g}{\bar{Z}_i + \bar{Z}_g}\bar{U}_I + \frac{\bar{Z}_i}{\bar{Z}_i + \bar{Z}_g}\bar{U}_g \quad (5\text{-}5)$$

$$\begin{cases} \bar{U}_{pcc} = \bar{U}_g + \bar{Z}_g \cdot \bar{\imath} \\ \bar{U}_{pcc} = \bar{U}_i - \bar{Z}_i \cdot \bar{\imath} \end{cases} \quad (5\text{-}6)$$

From (5-5), we can see that the voltage measured at the point of common coupling is a combination of both voltages where the source having the highest impact at the PCC is the one with the least impedance between its source and the PCC. If the inverter impedance is small compared to that of the grid, the inverter will most influence the voltage at the PCC and vice versa. In general, the grid impedance is considerably small so the voltage measured at the PCC is very close to the grid voltage. Figure 5-27 depicts an example of a space vector representation of the variation of $\bar{U}_{pcc}$ in function of the coupled voltages sources and their impedances. The lower the amplitude of grid impedance $\bar{Z}_g$ compared to that of the inverter $\bar{Z}_i$, the closer $\bar{U}_{pcc}$ is to the grid's voltage $\bar{U}_g$. This is also reversely true for the Inverter and its impedance.

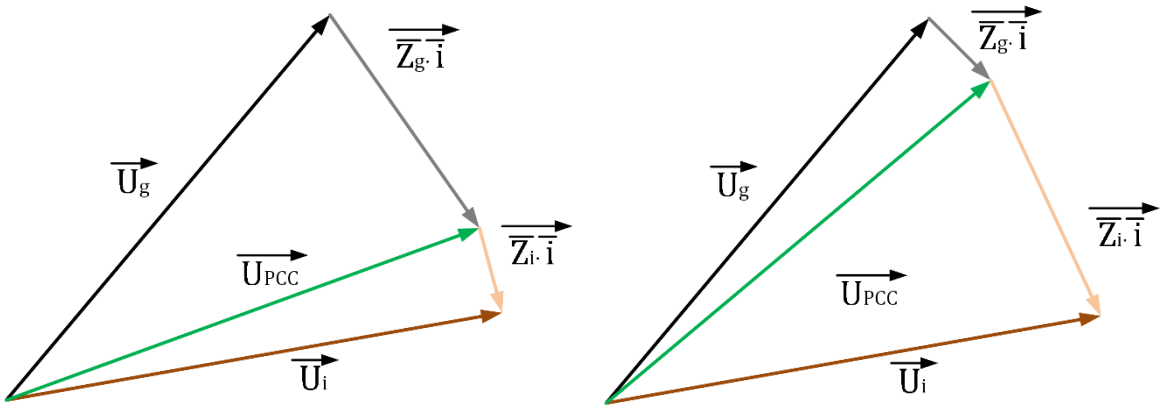


Figure 5-27: Instantaneous Vector Representations of Two Coupled Voltages Sources

The magnitude of the voltage at the PCC can be easily deduced from the grid and inverter voltage and impedances on the one hand. The phase angle compared to that of the inverter is, on the other hand, dependent on not only the magnitudes of the voltages and the global impedances but also on each source resistance and inductance.

When the voltage is computed in the dq-frame of the inverter,

$$U_{d_{pcc}} + i \cdot U_{q_{pcc}} = \frac{\bar{Z}_g}{\bar{Z}_i + \bar{Z}_g}\left(U_{d_i} + i \cdot U_{q_i}\right) + \frac{\bar{Z}_i}{\bar{Z}_i + \bar{Z}_g}\left(U_{d_g} + i \cdot U_{q_g}\right) \quad (5\text{-}7)$$

$$Z_i = R_i + i \cdot X_i; Z_g = R_g + i \cdot X_g \quad (5\text{-}8)$$

$$with\ \alpha = \frac{R_i}{X_i}; \beta = \frac{X_g}{X_i};\ \gamma = \frac{R_g}{X_g}$$

$$\frac{\bar{Z}_g}{\bar{Z}_i + \bar{Z}_g} = \frac{R_g + i \cdot X_g}{R_i + R_g + i(X_i + X_g)} = \frac{\alpha\beta X_i + i \cdot \alpha\beta\gamma X_i}{\alpha X_i + \alpha\beta X_i + i(X_i + \alpha\beta\gamma X_i)} = \frac{\alpha\beta + i \cdot \alpha\beta\gamma}{\alpha + \alpha\beta + i(1 + \alpha\beta\gamma)}$$

$$\frac{\bar{Z}_i}{\bar{Z}_i + \bar{Z}_g} = \frac{R_i + i \cdot X_i}{R_i + R_g + i(X_i + X_g)} = \frac{\alpha X_i + i \cdot X_i}{\alpha X_i + \alpha\beta X_i + i(X_i + \alpha\beta\gamma X_i)} = \frac{\alpha + i}{\alpha + \alpha\beta + i(1 + \alpha\beta\gamma)}$$

$$\begin{cases} \dfrac{\bar{Z}_g}{\bar{Z}_i + \bar{Z}_g} = \dfrac{\alpha\beta + i \cdot \alpha\beta\gamma}{\alpha + \alpha\beta + i(1 + \alpha\beta\gamma)} \\ \dfrac{\bar{Z}_i}{\bar{Z}_i + \bar{Z}_g} = \dfrac{\alpha + i}{\alpha + \alpha\beta + i(1 + \alpha\beta\gamma)} \end{cases} \quad \left(\alpha = \frac{R_i}{X_i}; \beta = \frac{X_g}{X_i}; \gamma = \frac{R_g}{X_g}\right) \qquad (5\text{-}9)$$

5.5.1.2 PCC Voltage at Equal Resistance and Inductances Ratio

This parametric equation has been implemented in MATLAB. The Figure 5-28 illustrates how the voltage at the PCC is influenced by the inverter and grid impedances. The calculations have been performed for the following configuration: the inverter voltage magnitude is 220V, the inverter impedance is set to 0.08Ωand the phase angle difference between the grid and the inverter voltages is 0.1 rad. In the first scenario, α and γ are equal to 1/8. This means that the ratio of the inverter inductance to its resistance is the same for the grid. Figure 5-28 shows how the ratio of the grid impedance to that of the inverter influences the voltage at the PCC compared to the grid voltage. It can be noticed that, if the magnitude of the grid voltage is equal to that of the inverter, the voltage at the PCC will have the same amplitude as the grid even if the impedance ratio varies. It can also be noticed that the U_{pcc} gets closer to the grid voltage in magnitude and in phase as the grid impedance decreases. The phase difference is less than 15% and the magnitude difference less than 5% when the grid impedance is 8 times less than that of the inverter. The phase difference nears 90% when the grid impedance is 8 times greater and the magnitude difference is between 17% and 30% when the grid voltage is 25% greater and 25% less than the inverter voltage respectively. When both impedances are equal, the phase difference is 50% when both magnitudes are equal and varies between about 60% to 40% as the grid magnitude varies by -25% to +25% compared to the inverter amplitude.

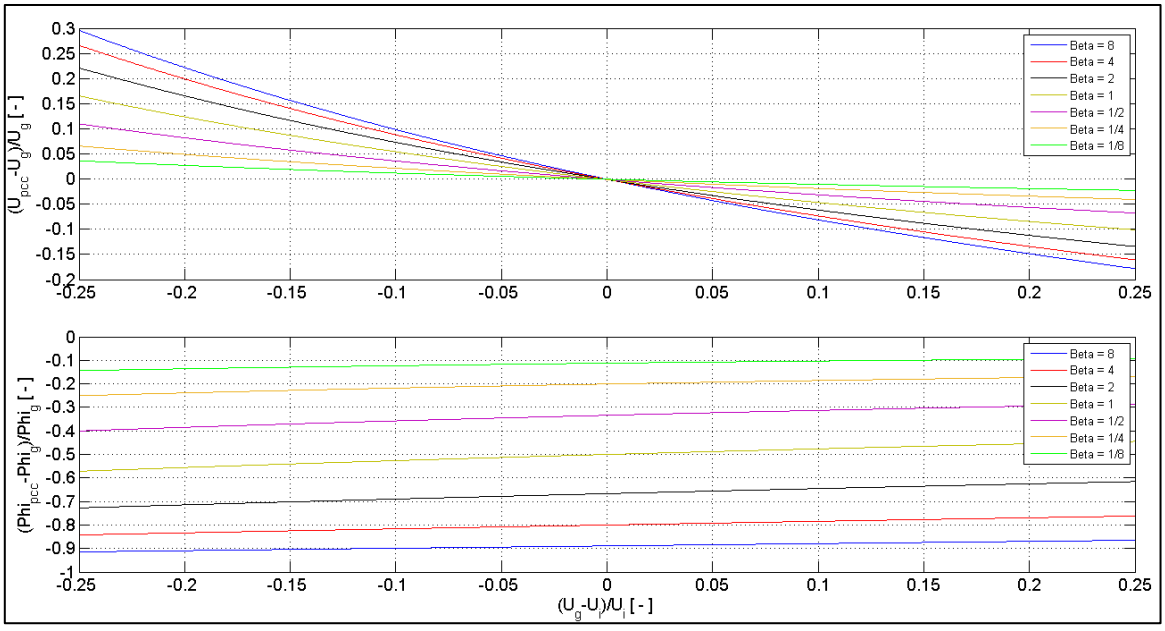


Figure 5-28: PCC's Voltage vs Grid Voltage with Identical Inverter and Grid Impedance Angle

5.5.1.3 PCC Voltage by Different Resistance and Inductance Ratio

In a more realistic case, Figure 5-29 depicts how the voltage at the PCC is influenced by the ratio of the inverter resistance to the inverter inductance α and the ratio of the grid resistance

to the grid inductance γ are not equal. It shows that the PCC voltage magnitude is not as much affected as the phase angle. On the one hand, the magnitude is mostly affected by the global impedance ratio between the inverter and the grid as previously seen on Figure 5-29. On the other hand, the phase angle of the voltage at the PCC is very sensitive to these characteristic unbalance. The phase angle difference varies proportionally to the impedances ratio as long as the resistance to inductance ratios are the same. The largest difference appears when a mostly resistive inverter ($\alpha > 1$) is coupled to a mostly inductive grid ($\gamma < 1$) or when a mostly inductive inverter ($\alpha < 1$) is coupled to a mostly resistive grid ($\gamma > 1$).

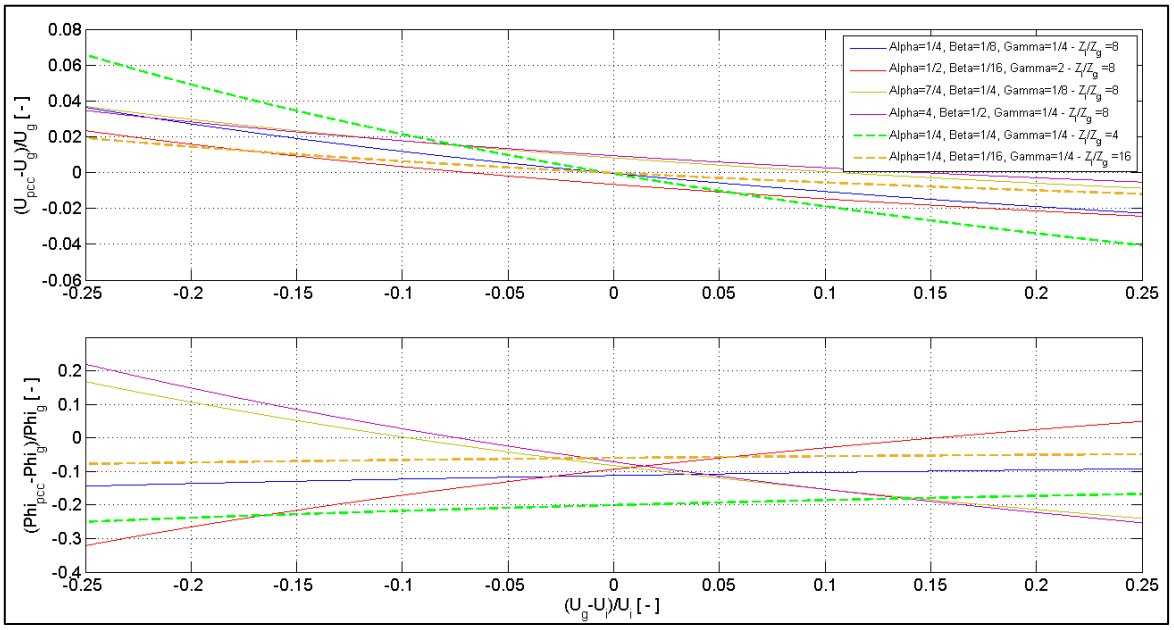


Figure 5-29: PCC's Voltage vs Grid Voltage with Various Inverter and Grid Impedance Angle but Same Impedance Ratio

5.5.1.4 Conclusion

For two coupled power grids, the voltage obtained at the PCC results from a strong interaction between both voltages. The resistance and inductance ratio from one voltage source to the second are the key parameters determining how one source affects the PCC voltage. If the voltage sources are equal (in magnitude and phase angle), the impedances effects disappear since the PCC voltage is also equal to that of the sources. The source with the least impedance has the greatest impact on the PCC voltage magnitude. The phase angle measured at the PCC is affected not only by the impedance magnitude ratio but also by the resistance and inductance ratio of one source to another. Nevertheless, the PCC remains a good point to detect any change in the system, even if the detected changes are amplified or attenuated at the PCC.

5.5.2 Synchronisation and Coupling

5.5.2.1 PLL-based Synchronisation

The working principle of the synchronisation and coupling is depicted in Figure 5-30. It is composed of one magnitude and phase angle controller. The grid voltage is measured and its magnitude and phase angle are determined through a PLL. A second PLL is used to detect the amplitude and the phase angle of the generated voltage at the output of the passive filter. The voltage magnitude controller brings the generated magnitude to its set-point value, which is the grid voltage magnitude and the phase angle controller, corrects the phase angle of the generated voltage so that it is equal to that of the grid voltage. The maximum allowed

magnitude difference is 2 volts and the maximum phase angle difference is 0.01 rad. Once both controllers have reached the set-points and remain stable for a given time (a couple of milliseconds), the synchronisation is complete. This synchronisation status is then used as the release of the switch-on signal to the coupling relay that connects the inverter unit with the main grid. The main grid is modelled by a three-phase voltage source in series with an internal resistance and inductance. Their values are chosen very low (compared to the existing real grid) to make it sensitive to harmonic distortion caused by non-linear loads. The grid resistance is 0.04 Ω and its inductance is 4mH. The nominal frequency and the phase-to-phase voltage RMS value are respectively 50 Hz and 400V.

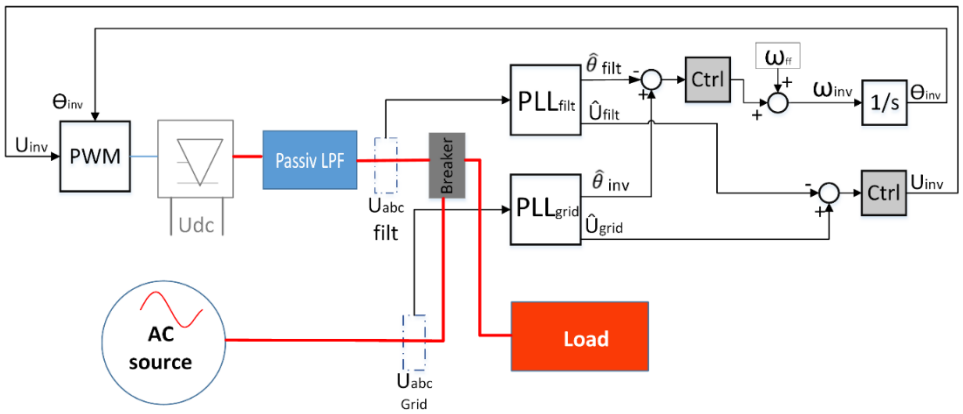


Figure 5-30: PLL-based Synchronisation of the Inverter to an AC Voltage Source

The Figure 5-31 illustrates this synchronisation process. The magnitude of the inverter voltage increases, while its phase angle nears that of the grid voltage. Once the synchronisation is terminated, the two systems are coupled and the phase error and the instantaneous voltage difference directly drop to zero.

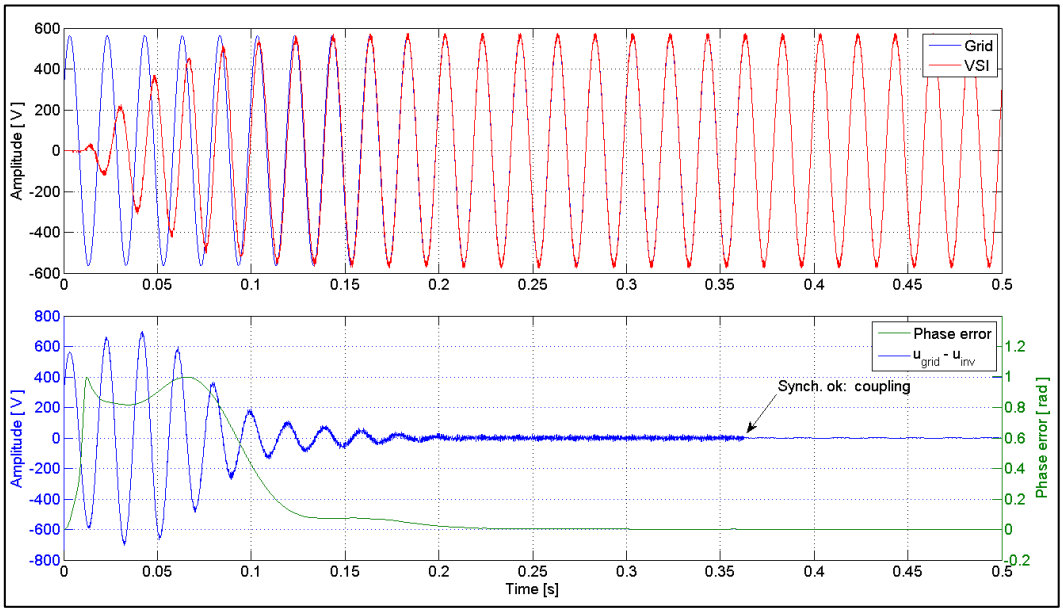


Figure 5-31: Magnitude and Phase Synchronization Process Using PLLs

5.5.2.2 Synchronisation of the Voltage dq Components in the Inverter Frame

Another synchronisation process can be realised without using the virtual coordinates of the PLLs but based on the already known inverter coordinates. This is illustrated in Figure 5-32.

The direct and quadrature components of the voltages of the grid, as well as that of the filter output, are calculated in the same rotating frame, the inverter frame. The magnitude of the filter output voltage is separately controlled to match that of the measured grid voltage. The VSI output and grid voltages dq components in the inverter reference frame are expressed in (1) where: $\widehat{U}_f$ and $\widehat{U}_g$ are the inverter filtered and grid voltage magnitude. θ_{inv}, θ_f and θ_g are the phase-angle of the inverter reference signal, the filtered VSI voltage and the grid voltage respectively.

$$\begin{cases} U_{d_f} = -\widehat{U}_f \sin(\theta_{inv} - \theta_f) \\ U_{d_g} = -\widehat{U}_g \sin(\theta_{inv} - \theta_g) \\ U_{q_f} = \widehat{U}_f \cos(\theta_{inv} - \theta_f) \\ U_{q_g} = \widehat{U}_g \cos(\theta_{inv} - \theta_g) \end{cases} \quad (5\text{-}10)$$

As the goal is to reach a zero phase-shift between the voltages, the inverter frequency is controlled so that the grid and the inverter direct components are equal, using the phase-shift representative value given by

$$e_\theta = \left(U_{d_f} \times U_{q_g} - U_{q_f} \times U_{d_g}\right) \quad (5\text{-}11)$$

(5-10) into (5-11) leads to,

$$e_\theta = \widehat{U}_f \cdot \widehat{U}_g \sin(\theta_f - \theta_g) \quad (5\text{-}12)$$

Equation (5-12) will be zero only when the VSI voltage phase-angle θ_f is equal to that of the grid voltage θ_g. This leads to $U_{d_f} = U_{d_g}$ when both voltage magnitudes are equal. For small phase-shift values, (5-12) can be linearized to

$$e_\theta = \widehat{U}_f \cdot \widehat{U}_g(\theta_f - \theta_g) \quad (5\text{-}13)$$

This is similar to the controlled voltage value in the SFR-PLL [92]. The difference here is that the computed phase-shift is not between one measured signal and the internal PLL frame but between two measured voltages to be synchronised. e_θ represents the value that has to be regulated to zero in order to ensure a zero phase-shift between the voltages. It is important to start the control of the voltage magnitude before that of the phase because the phase control is strictly dependent on the stability of the voltages magnitudes. Any disturbance or oscillatory or linear transient caused by the magnitude control strongly affects the phase control since it is based on real voltages values.

Similar to the previous synchronisation method using the PLLs, the coupling relay is turned on after a time delay, where the phase and amplitude controllers should remain within certain limits. The Figure 5-33 shows the results of this synchronisation process. In order to avoid useless calculations by the phase controller, the magnitude of the inverter is first activated and then the phase controller starts only after the magnitude difference is less than 30V. Starting the phase controller too early is not necessary since the phase control is strongly bound to that of magnitude. Therefore, it will be stable only after the magnitude control reaches its steady state.

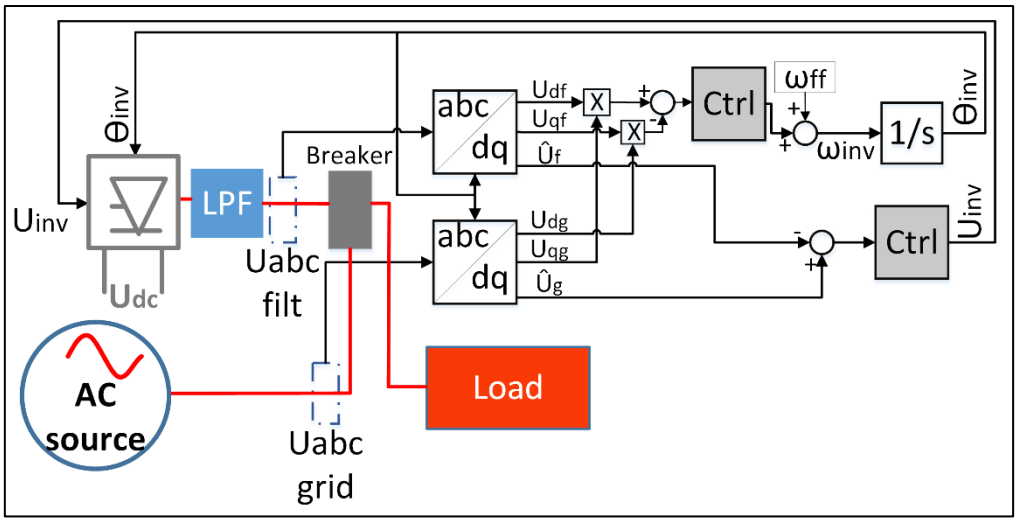


Figure 5-32: Inverter dq Frame-based Synchronisation of the Inverter to an AC Voltage Source

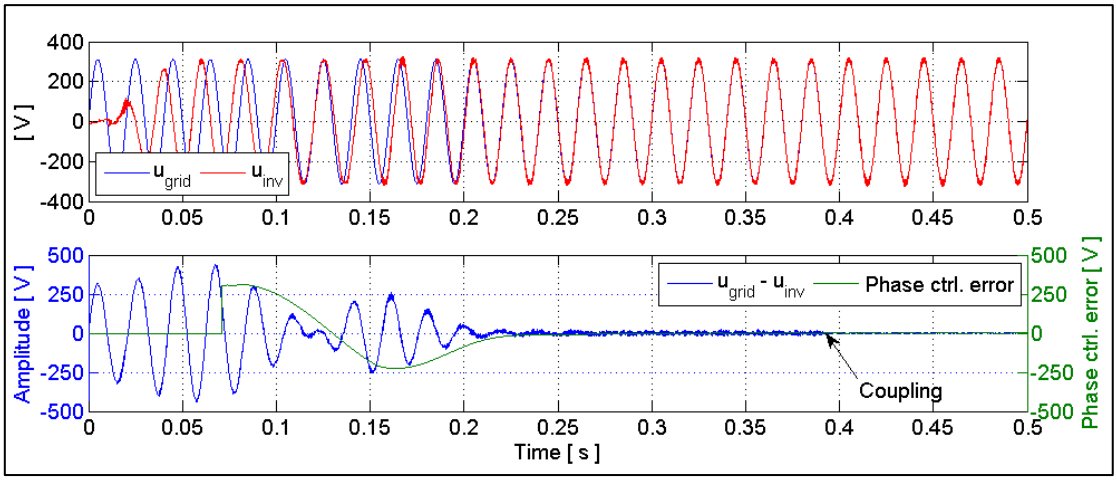


Figure 5-33: Inverter-Grid Synchronisation Process in the Inverter frame

The Figure 5-34 shows that the exchanged power directly after the coupling is not zero but remains quite low. This is due to the imperfect voltage output of the passive RLC filter and also to the synchronisation amplitude and phase angle error, which are considerably small non-zero values. The most critical aspect is the power oscillations appearing (see 5.5.3).

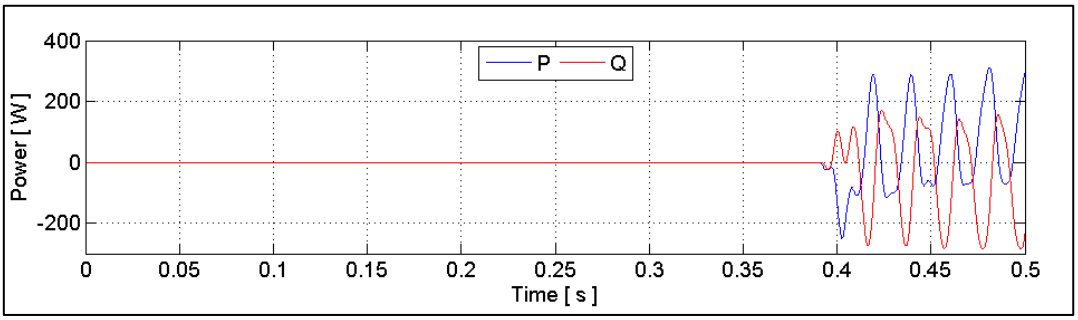


Figure 5-34: Power Flow after Coupling

5.5.2.3 Synchronization of Distorted Voltage Sources

The voltage distortions have a considerable impact on the signal identification algorithms. The calculated direct and quadrature components, as well as the phase angle, might oscillate more or less depending on the degree of distortion. This means that any attempts of

synchronisation will fail unless the tolerance limits are increased so that the oscillations caused by the harmonics remains within the tolerance range. The perfect method of synchronisation on a distorted voltage source consists of generating not only the fundamental voltage but also the existing harmonics. Comparable to the harmonic compensation methods, the goal of the harmonics controllers is to generate harmonics that match in magnitude and phase with those contained in the distorted grid voltage. Nevertheless, this method requires twice the number of components for the harmonics detection. Since the harmonics voltages magnitudes are generally small compared to the fundamental voltage, only the fundamental waves are synchronised. As depicted in Figure 5-35, the measured voltages must first be filtered to extract only their fundamental signals. The synchronisation process is then performed ignoring the eventual harmonics. This results in a power flow right after coupling due to the harmonics voltages but it remains quite low.

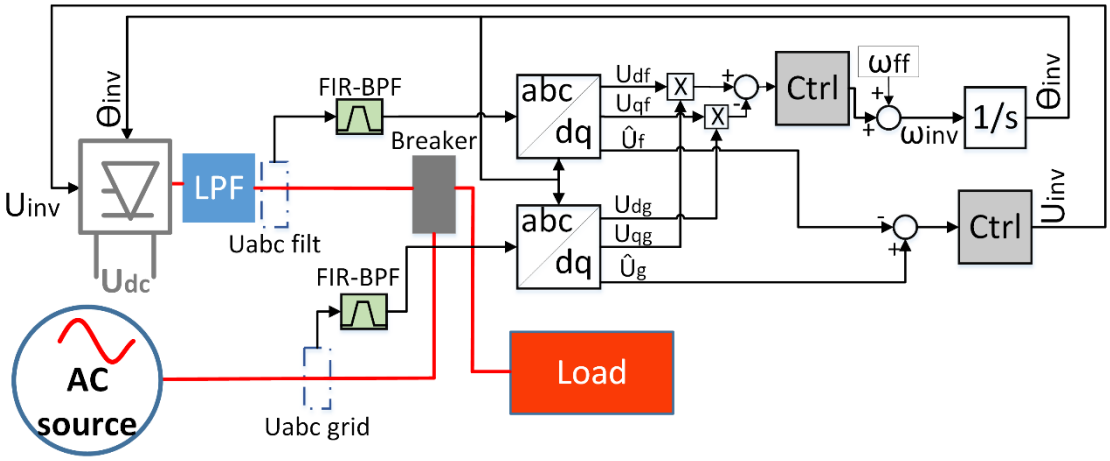


Figure 5-35: Inverter Frame-based Synchronization with Distorted Grid Voltages

The Figure 5-36 depicts the synchronisation process of the inverter to a distorted grid voltage. Since only the fundamental component of each voltage is taken into consideration, the magnitude and phase control is identical to the previous ones. The main disparity is the level of active and reactive power exchanged after the coupling occurred. Due to the harmonic distortion, the instantaneous voltage difference is much higher than that obtained for a non-distorted grid voltage. Thus, the active and reactive power flow is greater.

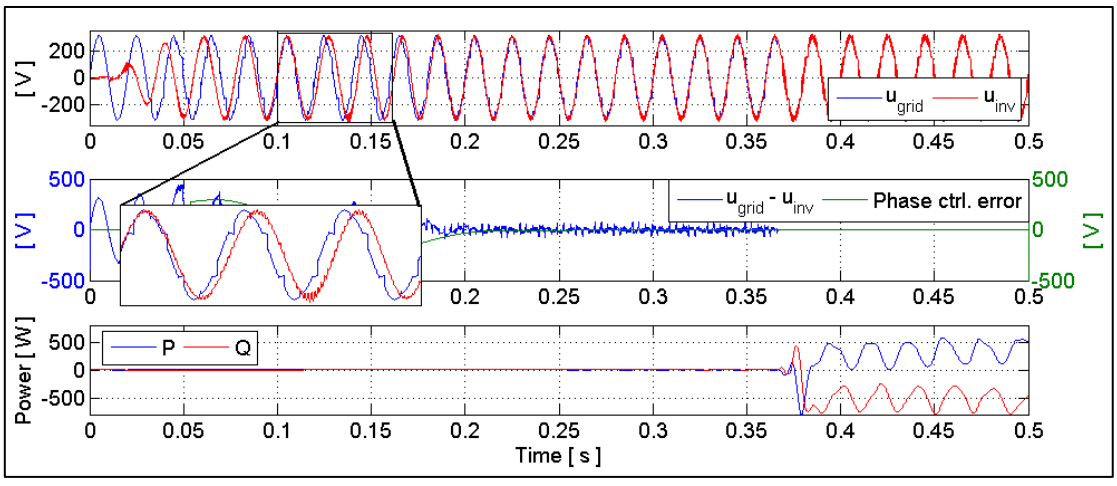


Figure 5-36: Inverter Synchronisation Process in the Inverter Frame and Power Flow after Coupling

5.5.3 Current Flow after Coupling

Are the oscillations observed on the computed values of the active and reactive power caused by the residual harmonics voltage? As the power flow is mainly due to the fundamental voltage and current, the power calculation is based only on the 50Hz waves. Therefore, the measured currents are also filtered using a 50Hz band-pass FIR filter. The harmonic currents are ignored by the main power flow control but will be controlled by the voltage harmonic compensation. However, simulations showed that the currents are asymmetrical and this is the main cause of the oscillating fundamental powers. Three different systems of controlled voltage sources are compared. The first consists of a power inverter controlled by the intersection method, the second one is controlled using the space vector modulation and the last is simply an ideal voltage source whose voltage output is also filtered through the same passive filter as the one used for filtering the PWM voltages. They are synchronised to the same grid and the asymmetry of the current leading to oscillating power are compared.

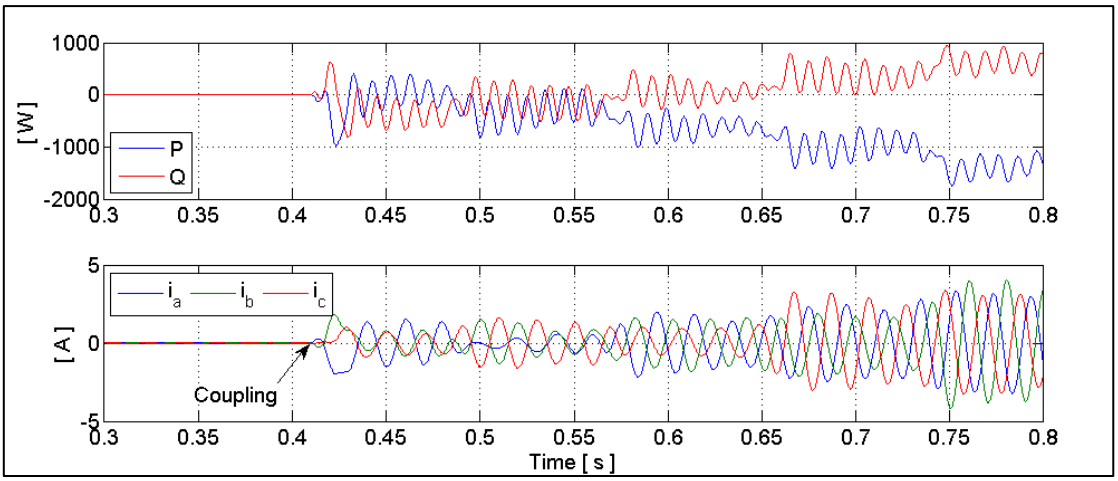


Figure 5-37: Power Flow after Coupling with the Space Vector Modulation

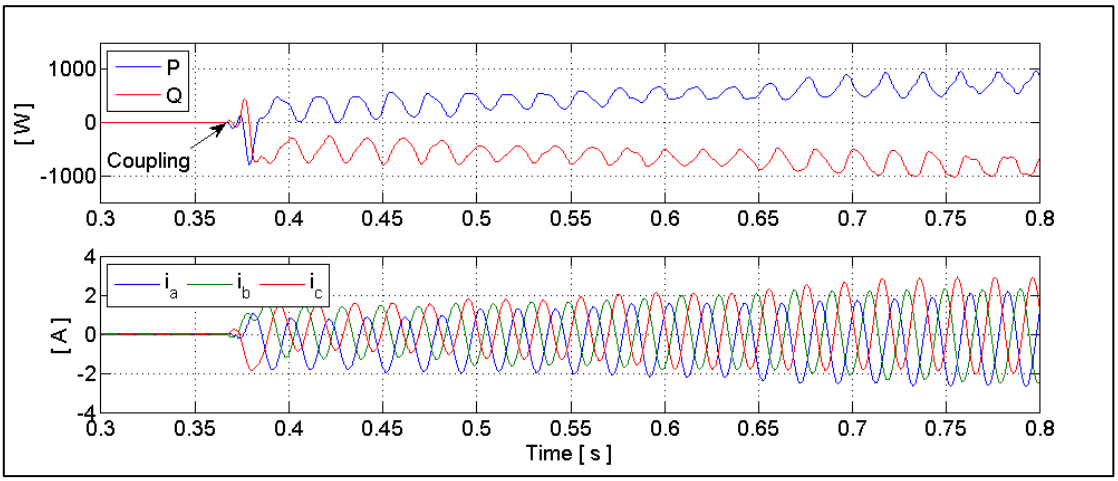


Figure 5-38: Power Flow after Coupling with the Intersection Method

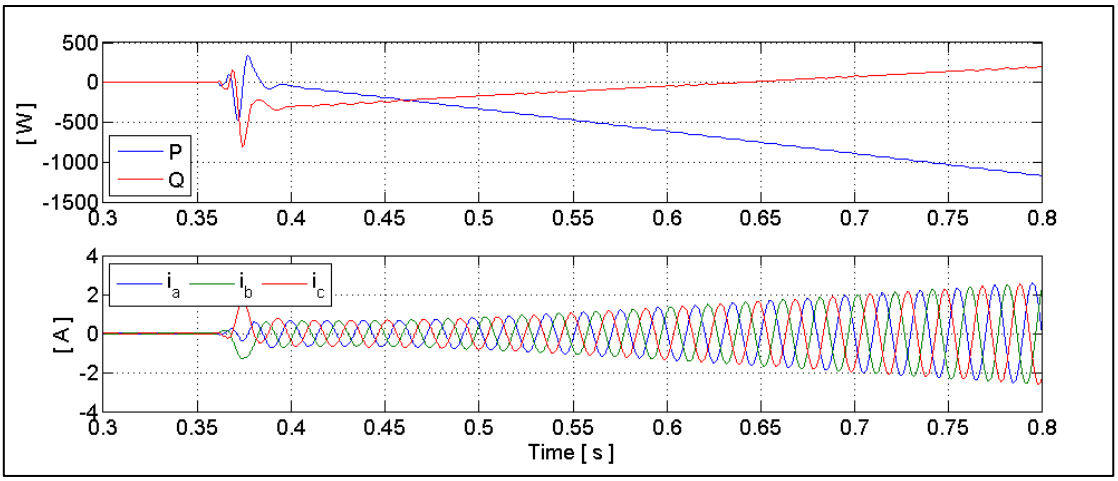


Figure 5-39: Power Flow after Coupling of Two Ideal Sources

The results show that the PWM generation methods are similar except that the unbalance of the phase currents are maybe different in appearance. This unbalance disappears completely when the ideal voltage sources are used except during the transient phase. The computed active and reactive power presents no oscillations. A further investigation has been done to verify if, the high-frequency voltages still contained in the filtered output voltage of the PWM is the cause of the current unbalance after the coupling. A controlled distorted voltage source is generated (50Hz and 11th harmonic) and synchronised to the second (grid) voltage source. Once coupled, there are oscillations during the transient phase that decrease with the time as the currents converge towards the steady and balanced state. This means the remaining harmonic content of the filtered PWM may not be the cause of the current unbalance.

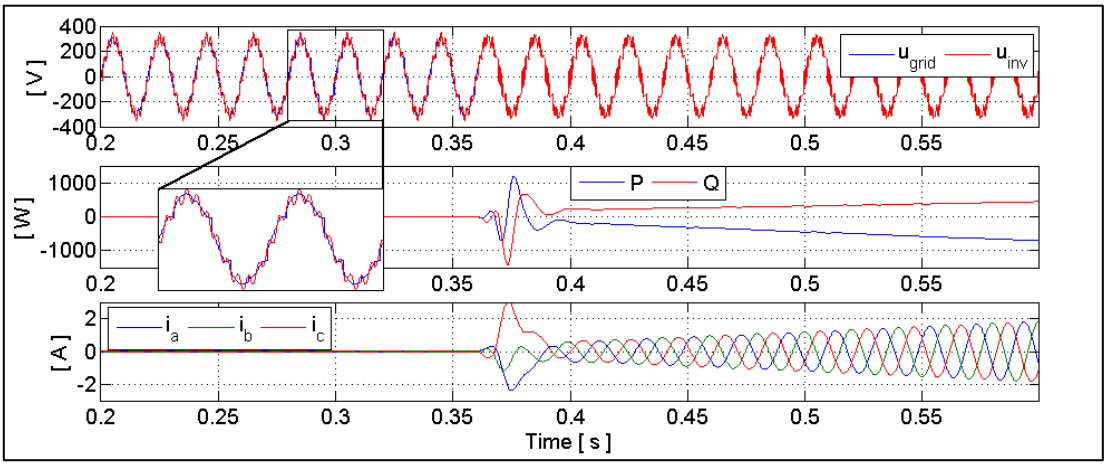


Figure 5-40: Synchronisation of a Distorted Ideal Voltage Source with the Grid and Power Flow after Coupling

5.5.4 Conclusion

The output voltage of the inverter can be easily synchronised to a grid voltage with or without harmonics content. The synchronisation process based on the PLLs requires more computational power than the method where the grid and PWM filtered voltages are decomposed into their direct and quadrature component into the inverter frame, which is perfectly known. This last method provides a further use since the comparison of the direct components can also be interpreted as the phase difference between the voltages. It can also give the information about the phase shift due to the passive filter (assuming there is no amplitude drop when the filter is not loaded). The appearing unbalance in the measured current affects the computed power. A numeric low-pass filter can help to reduce the impact

of the oscillating power on the power flow control. The numerical low-pass filter should have a good compromise between the response time and the filtering efficiency in order to avoid modifying the dynamic of the control loop.

5.5.5 Power Inverter as a Grid Power Support

Once the inverter system is coupled to the grid, the standard voltage magnitude and phase regulation is no longer applicable since the voltage characteristic of the interconnected system is imposed by the grid, unless the grid impedance is considerably low, so that it can be easily influenced by power units connected to it. The electrical values that indicate if the both systems are still perfectly synchronised are the active and reactive power supplied by the inverter into the grid. Any of these power component changes whenever any desynchronization occurs. This could be a magnitude and/or a frequency change, i.e. a phase difference. In order to control independently the active as well as the reactive power transfer, that is required to support the grid or due to a grid state variation, the key factor is the knowledge of the overall impedance of the electrical circuit between the power units.

The following sub-chapters show how to estimate the system impedance in order to control the active and reactive power flow delivered by the inverter.

5.5.5.1 Proposed Online Electrical Circuit Impedance Estimation

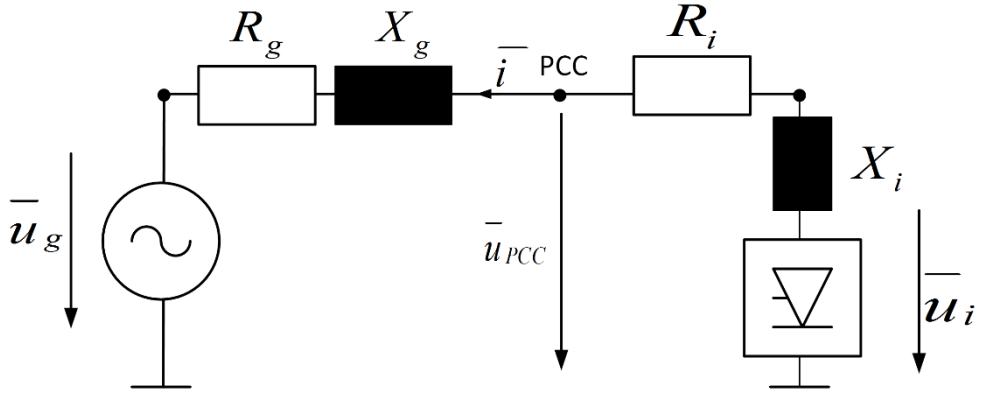


Figure 5-41: Model of a Grid-tied Power Inverter

The system shown in Figure 5-41 is composed of a power inverter, whose output is connected to a low-pass inductive-capacitive filter (LC-filter) that will filter the high frequency Pulse Width Modulation (PWM), so that the output voltage of the LC-filter is a 50Hz signal with a very low total harmonic distortion (THD). Once the grid and the LC-filter output voltages are synchronised and coupled, the voltage at the point of common coupling (PCC) is calculated in the well-known orthogonal and rotating (dq) reference frame of the inverter. The phase-shift λ between the voltage at the PCC and the inverter voltage is deduced from the computed voltage direct component and the voltage magnitude at the PCC. The magnitude difference ΔU between the grid voltage and that of the inverter is set to zero at the coupling instant and is estimated to any positive or negative voltage variation applied for the inverter control (after the coupling occurred). The drawn current is also measured and decomposed in its direct and quadrature component in the inverter dq frame. The exchanged active and reactive power, P and Q respectively, are computed as a response to the phase-shift and/or the magnitude difference variations of the voltages as well as to the grid conductance and susceptance as shown in (5-21). These grid characteristics are therefore computed through an inverse matrix

having as parameters λ, ΔU and the synchronisation voltage of the inverter. Since the grid conductance and susceptance do not change abruptly, the computed values are numerically filtered in order to eliminate the transient power oscillations that could appear, when the control parameters (λ, ΔU) change. The estimated conductance and susceptance are then used to estimate the grid resistance and inductance as frame rotation angle, where the decoupled regulation of the active and reactive power can then be performed. The powers controllers determine a new magnitude difference and phase angle applied onto the inverter's voltage through the PWM generator that can be a sine-triangle or a space vector modulation. The method can be implemented for a three-phase power grid as well as for a single-phase one. See paragraph 0 for a detailed flowchart.

Let us consider the generated and controlled voltage U_2 of the inverter that has to be coupled to the grid voltage U_1:

$$\begin{cases} \overline{u_1} = \widehat{U}_1 \cdot e^{j\omega t} \\ \overline{u_2} = \widehat{U}_2 \cdot e^{j\omega t} \cdot e^{-j\lambda} \end{cases} \quad (5\text{-}14)$$

Where:

λ is the phase difference between the grid voltage and the inverter-generated voltage.

$\widehat{U}_1$ & $\widehat{U}_2$ are the magnitudes of the grid and the inverter voltages respectively.

Since the relevant variables are the powers delivered by the power inverter, a current flow from the inverter into the grid is supposed positive.

The delivered current $\bar{\imath}$ flowing from the inverter to the grid through a resistive-inductive line (RL) is given by:

$$\bar{\imath} = \frac{\overline{u_2} - \overline{u_1}}{R + j\omega L} = \frac{\widehat{U}_2 \cdot e^{j\omega t} \cdot e^{-j\lambda} - \widehat{U}_1 \cdot e^{j\omega t}}{R + j\omega L} \quad (5\text{-}15)$$

$$\bar{\imath} = \left(\frac{R - j\omega L}{R^2 + (\omega L)^2}\right)\left(\widehat{U}_2 \cdot e^{-j\lambda} - \widehat{U}_1\right)e^{j\omega t}$$

$$\bar{\imath} = \left(\frac{R - j\omega L}{Z^2}\right)\left(\widehat{U}_2 \cos(\lambda) + j\widehat{U}_2 \sin(\lambda) - \widehat{U}_1\right)e^{j\omega t}$$

$$\bar{\imath} = \left(\frac{e^{j\omega t}}{Z^2}\right)\left[R\left(\widehat{U}_2 \cos(\lambda) - \widehat{U}_1\right) + \widehat{U}_2 \omega L \sin(\lambda) - j\left(\omega L\left(\widehat{U}_2 \cos(\lambda) - \widehat{U}_1\right) - R \cdot \widehat{U}_2 \sin(\lambda)\right)\right] \quad (5\text{-}16)$$

The apparent power $\bar{S}$ supplied by the inverter is given by

$$\bar{S} = \frac{1}{2}\overline{u_2} \cdot \bar{\imath}^* \quad (5\text{-}17)$$

$$\bar{S} = \frac{1}{2}\widehat{U}_2 \cdot e^{j\omega t} \cdot e^{-j\lambda}\left(\frac{e^{j\omega t}}{Z^2}\right)\left[R\left(\widehat{U}_2 \cos(\lambda) - \widehat{U}_1\right) + \widehat{U}_2 \omega L \sin(\lambda) - j\left(\omega L\left(\widehat{U}_2 \cos(\lambda) - \widehat{U}_1\right) - R \cdot \widehat{U}_2 \sin(\lambda)\right)\right]$$

$$\bar{S} = \frac{1}{2}\left(\frac{1}{Z^2}\right)\left[R\left(\widehat{U}_2^2 \cos(\lambda) - \widehat{U}_1\widehat{U}_2\right) + \widehat{U}_2^2 \omega L \sin(\lambda) - j\left(\omega L\left(\widehat{U}_2^2 \cos(\lambda) - \widehat{U}_1\widehat{U}_2\right) - R \cdot \widehat{U}_2^2 \sin(\lambda)\right)\right] \cdot e^{j2\omega t} \cdot e^{-j\lambda} \quad (5\text{-}18)$$

The apparent power can be decomposed into the active and reactive power P and Q whose values are

$$\begin{cases} P = \frac{1}{2} \cdot \frac{1}{Z^2}\left[R\left(\widehat{U}_2^2 \cos(\lambda) - \widehat{U}_1\widehat{U}_2\right) - \widehat{U}_2^2 \omega L \sin(\lambda)\right] \\ Q = -\frac{1}{2} \cdot \frac{1}{Z^2}\left[\omega L\left(\widehat{U}_2^2 \cos(\lambda) - \widehat{U}_1\widehat{U}_2\right) - R \cdot \widehat{U}_2^2 \sin(\lambda)\right] \end{cases} \quad (5\text{-}19)$$

Because λ is very small, the equations can be approximated as follows:

$$\begin{cases} P = \frac{1}{2} \cdot \frac{1}{Z^2}\left[R\left(\widehat{U}_2^2 - \widehat{U}_1\widehat{U}_2\right) - \widehat{U}_2^2 \omega L\lambda\right] \\ Q = -\frac{1}{2} \cdot \frac{1}{Z^2}\left[-\omega L\left(\widehat{U}_2^2 - \widehat{U}_1\widehat{U}_2\right) - R \cdot \widehat{U}_2^2\lambda\right] \end{cases} \quad (5\text{-}20)$$

With $\Delta U = \widehat{U}_1 - \widehat{U}_2$ follows:

$$\begin{cases} P = \frac{1}{2} \cdot \frac{1}{Z^2}\left[-R\widehat{U}_2\Delta U - \widehat{U}_2^2 \omega L\lambda\right] \\ Q = -\frac{1}{2} \cdot \frac{1}{Z^2}\left[\omega L\widehat{U}_2\Delta U - R \cdot \widehat{U}_2^2\lambda\right] \end{cases} \rightarrow \begin{cases} P = \frac{1}{2} \cdot \frac{\widehat{U}_2}{Z^2}\left[-R\Delta U - \widehat{U}_2\omega L\lambda\right] \\ Q = \frac{1}{2} \cdot \frac{\widehat{U}_2}{Z^2}\left[-\omega L\Delta U + R \cdot \widehat{U}_2\lambda\right] \end{cases}$$

$$\begin{cases} P = \frac{1}{2} \cdot \widehat{U}_2\left[-\Delta U\frac{R}{Z^2} - \widehat{U}_2\lambda\frac{\omega L}{Z^2}\right] \\ Q = \frac{1}{2} \cdot \widehat{U}_2\left[-\Delta U\frac{\omega L}{Z^2} + \widehat{U}_2\lambda\frac{R}{Z^2}\right] \end{cases}$$

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \frac{1}{2}\widehat{U}_2\begin{bmatrix} -\Delta U & -\widehat{U}_2\lambda \\ \widehat{U}_2\lambda & -\Delta U \end{bmatrix}\begin{bmatrix} R/Z^2 \\ \omega L/Z^2 \end{bmatrix} \quad (5\text{-}21)$$

Thus

$$\begin{bmatrix} R/Z^2 \\ \omega L/Z^2 \end{bmatrix} = \frac{2}{\widehat{U}_2} \cdot \frac{1}{(\Delta U)^2 + \lambda^2\widehat{U}_2^2}\begin{bmatrix} -\Delta U & \widehat{U}_2\lambda \\ -\widehat{U}_2\lambda & -\Delta U \end{bmatrix}\begin{bmatrix} P \\ Q \end{bmatrix} \quad (5\text{-}22)$$

$$\begin{bmatrix} R/Z^2 \\ \omega L/Z^2 \end{bmatrix} = \frac{2}{\widehat{U}_2} \cdot \frac{1}{(\Delta U)^2 + \lambda^2\widehat{U}_2^2}\begin{bmatrix} -\Delta U & \widehat{U}_2\lambda \\ -\widehat{U}_2\lambda & -\Delta U \end{bmatrix}\begin{bmatrix} P \\ Q \end{bmatrix}$$

$$= \frac{2}{\widehat{U}_2} \cdot \frac{1}{(\Delta U)^2 + \lambda^2\widehat{U}_2^2}\begin{bmatrix} -\Delta U & \widehat{U}_2\lambda \\ \widehat{U}_2\lambda & \Delta U \end{bmatrix}\begin{bmatrix} P \\ Q \end{bmatrix}$$

$$\begin{bmatrix} R/Z^2 \\ -\omega L/Z^2 \end{bmatrix} = \frac{2}{\widehat{U}_2} \cdot \frac{1}{(\Delta U)^2 + \left(\lambda\widehat{U}_2\right)^2}\begin{bmatrix} -\Delta U & \widehat{U}_2\lambda \\ \widehat{U}_2\lambda & \Delta U \end{bmatrix}\begin{bmatrix} P \\ Q \end{bmatrix} \quad (5\text{-}23)$$

R/Z^2 is defined as the conductance G of the electrical circuit and $-\omega L/Z^2$ as the susceptance B.

$$\begin{bmatrix} G \\ B \end{bmatrix} = \frac{2}{\widehat{U}_2} \cdot \frac{1}{(\Delta U)^2 + \lambda^2\widehat{U}_2^2}\begin{bmatrix} -\Delta U & \widehat{U}_2\lambda \\ \widehat{U}_2\lambda & \Delta U \end{bmatrix}\begin{bmatrix} P \\ Q \end{bmatrix} \quad (5\text{-}24)$$

With these values, the phase shift caused by the impedance can be found by computing the arctangent of the ratio of B/G.

To get the real impedance value, one can proceed as follows:

The values $G = R/Z^2$ and $B = -\omega L/Z^2$ computed in the simulation are now known.

$$G^2 + B^2 = \frac{R^2 + (\omega L)^2}{|Z|^4} = \frac{|Z|^2}{|Z|^4} = \frac{1}{|Z|^2}$$

The absolute value of the impedance is then deduced

$$Z = \sqrt{\frac{1}{G^2 + B^2}} \quad (5\text{-}25)$$

Knowing the value of the impedance as well as that of the conductance and the susceptance, R and ωL can be obtained as follows:

$$\begin{cases} R = G \cdot |Z|^2 \\ \omega L = B \cdot |Z|^2 \end{cases} \quad (5\text{-}26)$$

Depicted in Figure 5-42, a very simple micro-grid has been designed using ideal voltage sources. The voltage source VS1 is a static 50Hz voltage source with an amplitude of 200V and an impedance composed of the resistive and the inductive components R_g and L_g. A second voltage source is also providing a 50Hz AC voltage but for this device the, voltage magnitude and phase are controlled. Its impedance is made up of known components R and L. They are coupled through an ideal switch. The impedance estimator previously described is integrated and its goal is to determine the global impedance between the two voltage sources once they are coupled.

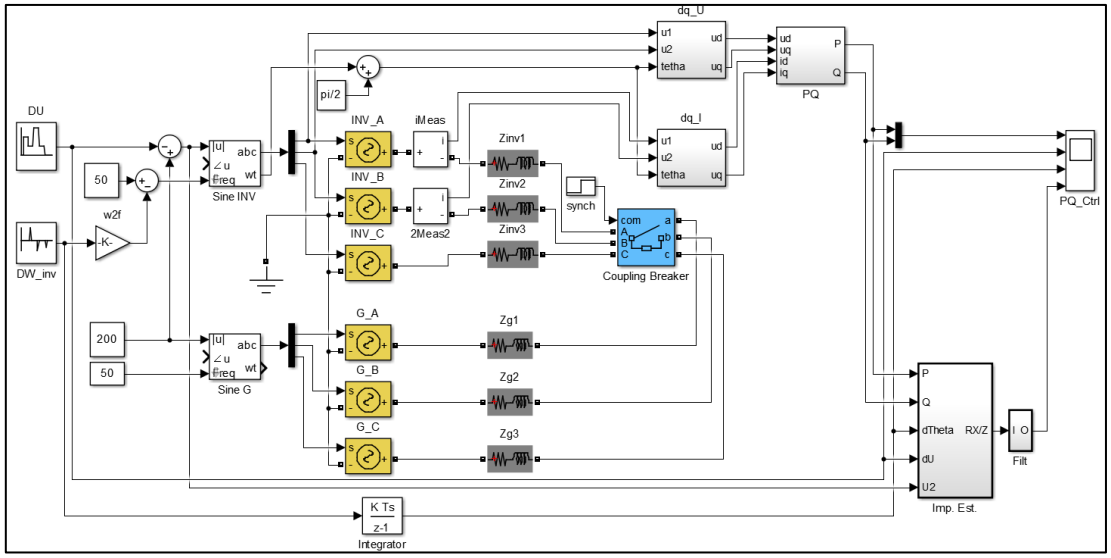


Figure 5-42: Simulink – Impedance Estimator for Two Coupled Ideal Voltage Sources

Scenario 1: The two sources are configured to be already synchronized from the beginning. The coupling occurs after 0.3 sec. The magnitude and the phase of the second voltage source are purposely changed multiple times in order to induce different value of the exchanged active and reactive power. The values of the resistances and inductances are as follows:

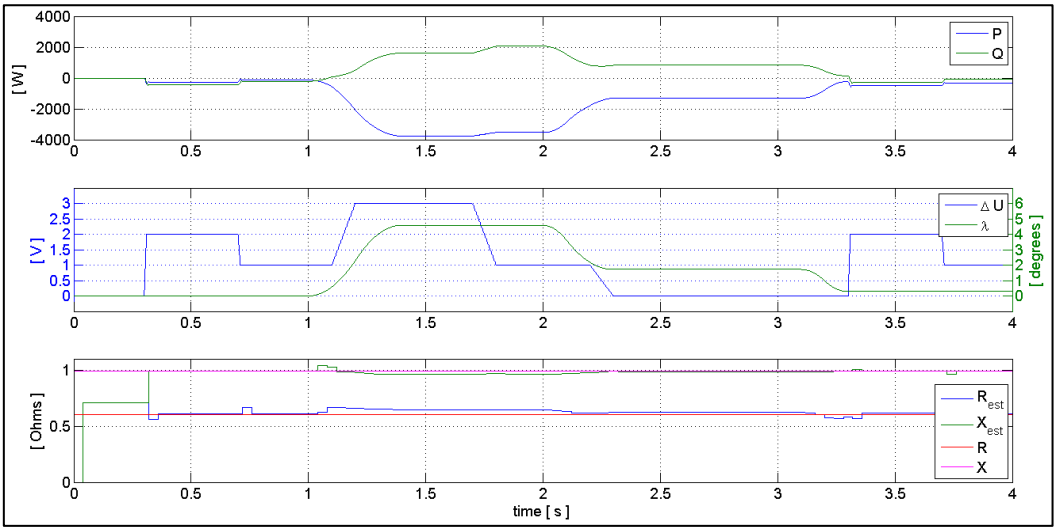


Figure 5-43: Impedance Estimation Performance for two Identical Coupled Grid

$R_g = R = 0.3\Omega, Lg = L = 1.58mH$. This means each impedance Z_g and Z are equal and are written $Z_g = Z = R_g + j\omega L$. Since the total impedance Zt is the sum of the impedances between the two sources, $Z_t = 2 \cdot R + 2 \cdot j\omega L$. This means that the estimator should be able to determine the value of 0.6 for the resistance and 2ωL, which is equal to 0.9927 for the inductance. The Figure 5-43 shows the identification performance of the estimator.

It can be noticed on the lower graph that the estimations are very close to the predicted values. The calculated values before the coupling are not valid since it is not possible to make any estimation without any power flow rate caused by the controlled change of one of the voltage sources. It is also interesting to notice that the estimation has a noticeable deviation during the transient phase of the process. This might be caused by the slightly delayed response of the system to the variation of the control parameters; the estimator delivers values based on power measurement that do not correspond to the amplitude difference and angle difference.

A second test scenario, **scenario 2**, has been performed with different values of the impedance.

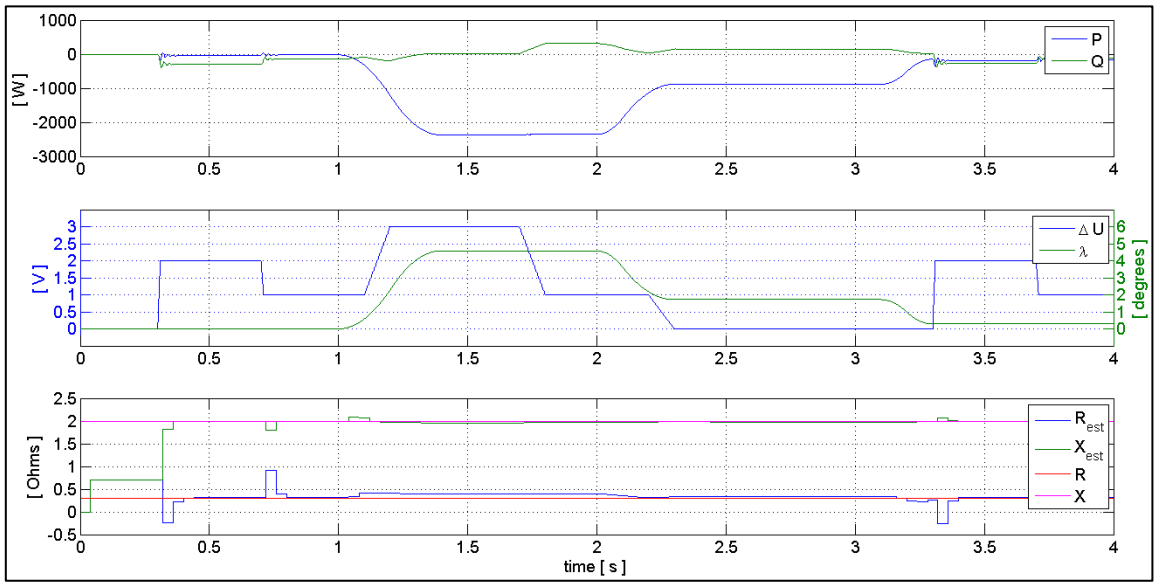


Figure 5-44: Impedance Estimation Performance for two Coupled Voltage Sources with Different Impedance

$R = .2\Omega, L = 1.58mH, R_g = 0.1\Omega \; and \; L_g = 3 \times 1.58mH$. The total impedance is then $Z_t = 0.3 + j\omega \times 4 \times 1.58.10^{-3} = 0.3000 + 1.9855j$. In addition, in this case, the estimator delivers very accurate values. This can then be integrated in the power flow control loop. Since the impedance changes very slowly and not much, the sampling frequency of the estimator can be quite low. In the depicted simulations, it had a frequency of 100Hz. Fast estimators can lead to bigger error for example when the system has not reached its final state after a magnitude or phase angle variation or both.

The Figure 5-44 shows, similarly to the results in Figure 5-43, that the estimator model is very sensitive to transient states. This means when the system has not yet reached its final response state after the change of a certain parameter. This is why the time delay of every element included in the data acquisition chain must be well known in order to minimise the estimation error.

A more realistic system (**scenario 3**) is made of a power inverter fed by a DC voltage. The pulsed output voltage of the inverter is filtered through a passive RLC filter and 50 Hz band-pass FIR filters are used on the measured voltages and currents in order to compute only the fundamental power. In order to quickly illustrate how sensitive the estimator model is toward delays, the system is reduced to ideal voltage sources as before (no filtered PWM voltage) but including the 50Hz band-pass FIR filters. The voltage and current FIR filter are identical and have 401 taps. With a sampling frequency of 20 kHz, the caused time delay is 10 ms. The Figure 5-45 depicts the difference between the estimated system resistance and inductance when the time delay is considered or not.

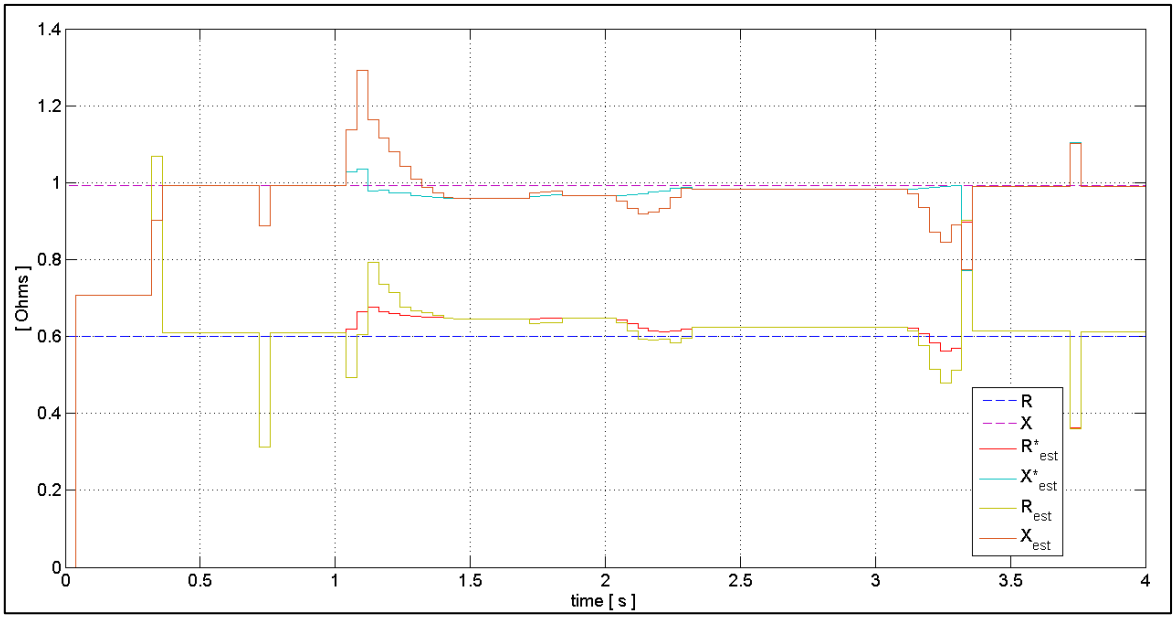


Figure 5-45: Impedance Estimation Performance with Input Value Matching Using a Transfer Delay

The value R and X are the real values, R_{est} and X_{est} are the estimated values without considering the FIR filters delays and R^*_{est} and X^*_{est} are the estimated values taking into consideration the FIR filters time delay. Figure 5-45 shows that adding the delay in the estimation reduces the sensitivity during the transient periods. In this open loop system, this might be neglected but in a regulated closed loop configuration, this improved stability is very important.

The estimation model has also been tested for the more realistic system, where the ideal controlled voltage is replaced by a passively filtered PWM voltage from a power inverter. An overview of the system is depicted in Figure 5-46 and the characteristics are as follows: the resistive-inductive grid has a voltage magnitude of 200 volts with an impedance $Z_g = 0.1 + \omega(3 \times 1.58)i$. The power inverter is controlled with a 15 kHz triangle carrier wave. The RLC low-pass filter is made of a resistance R_f, an inductance L_f and both are in parallel with a capacitor C_f with the value of $0.1\Omega, 1.58.10^{-3}H$ and $and\ 7.10^{-6}\ F$ respectively.

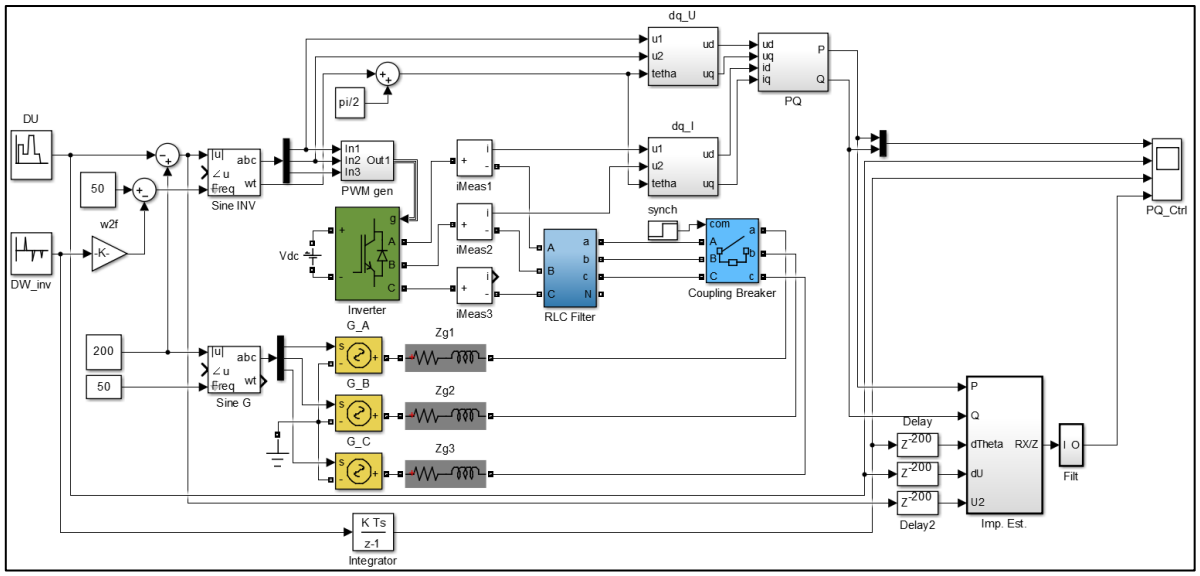


Figure 5-46: Simulink – Impedance Estimator Scheme for a Grid-tied Inverter

First, the Figure 5-47 shows the power flow generated by the same control parameter variation as in the previous systems. It is interesting to point out that the exchanged powers are similar to that in the case of the ideal voltage source. Despite the oscillations observed (due to the unbalanced current flow after coupling) on the active and the reactive power, the estimated values appear to be more stable when the apparent power is considerably higher compared to the level of oscillations. This is noticeable on Figure 5-48 for the period from 1 to 3.2 sec. In the cases where the oscillations are not negligible compared to the average value of the power, the estimations are very inaccurate and their sign can even be negative (depending on the values of the active and reactive power sampled at a given time for the calculation).

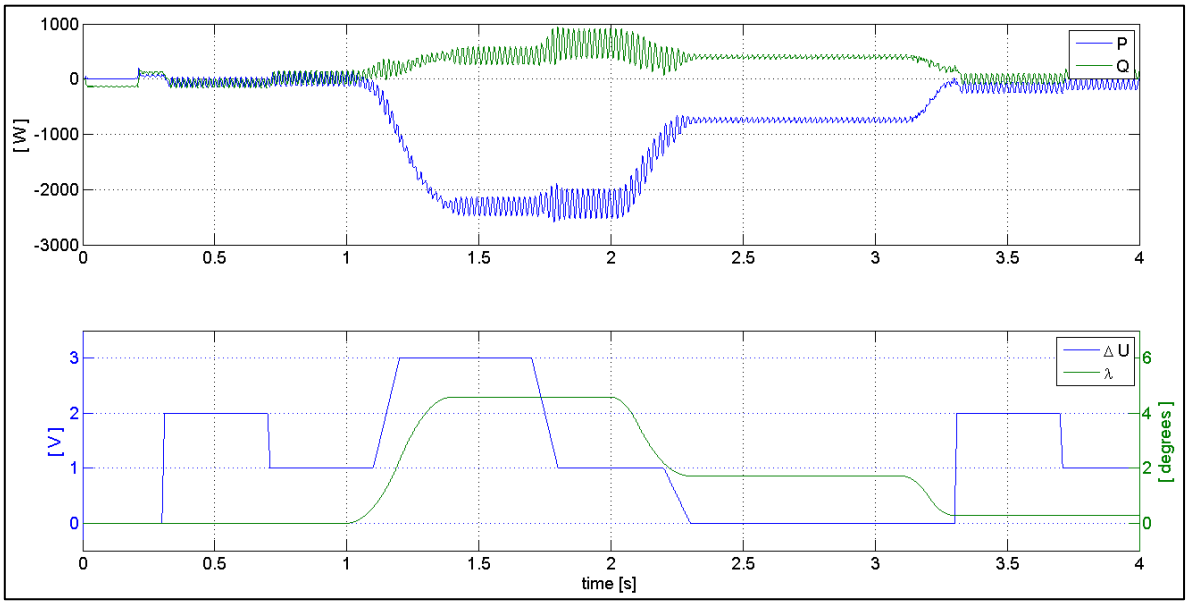


Figure 5-47: Power Flow between the Power Inverter and the Grid

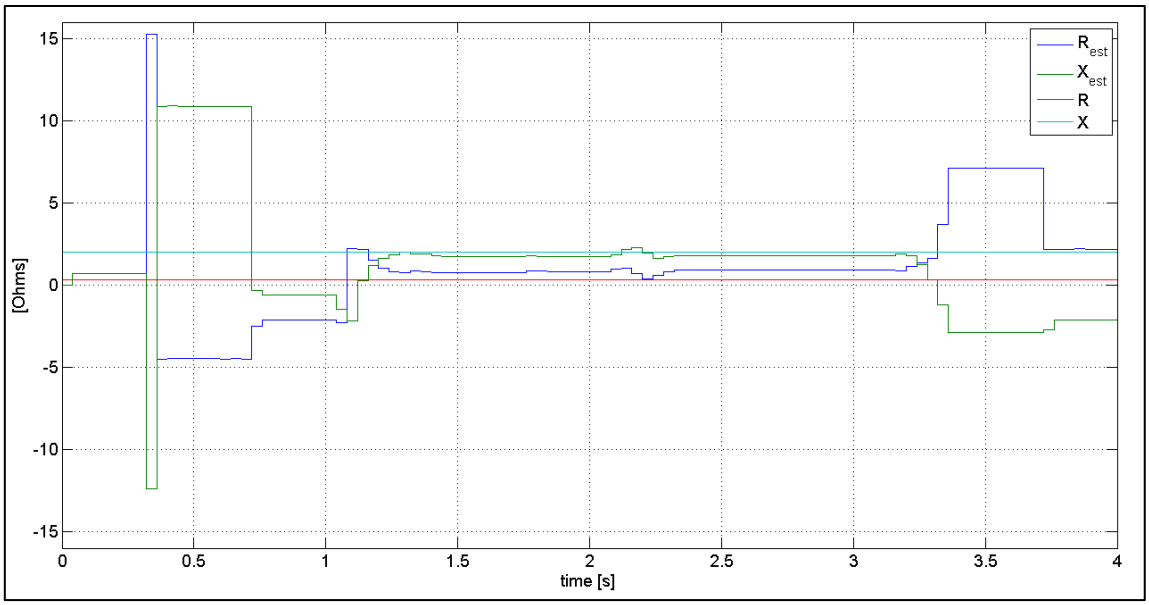


Figure 5-48: Impedance Estimation Performance for a Grid-tied Inverter

The impact of this power "ripple factor" is illustrated in Figure 5-49. The variation of the magnitude difference has been multiplied by 5 in order to achieve a higher power flow. The magnitude of the reactive power essentially has increased and the estimated resistance and inductance are more accurate. There is no negative value anymore; the estimated grid characteristic (mainly inductive) does not change over the time except for the short transient period. As seen before, the highest error level occurs when the apparent power is low (0.7sec-1.1 sec).

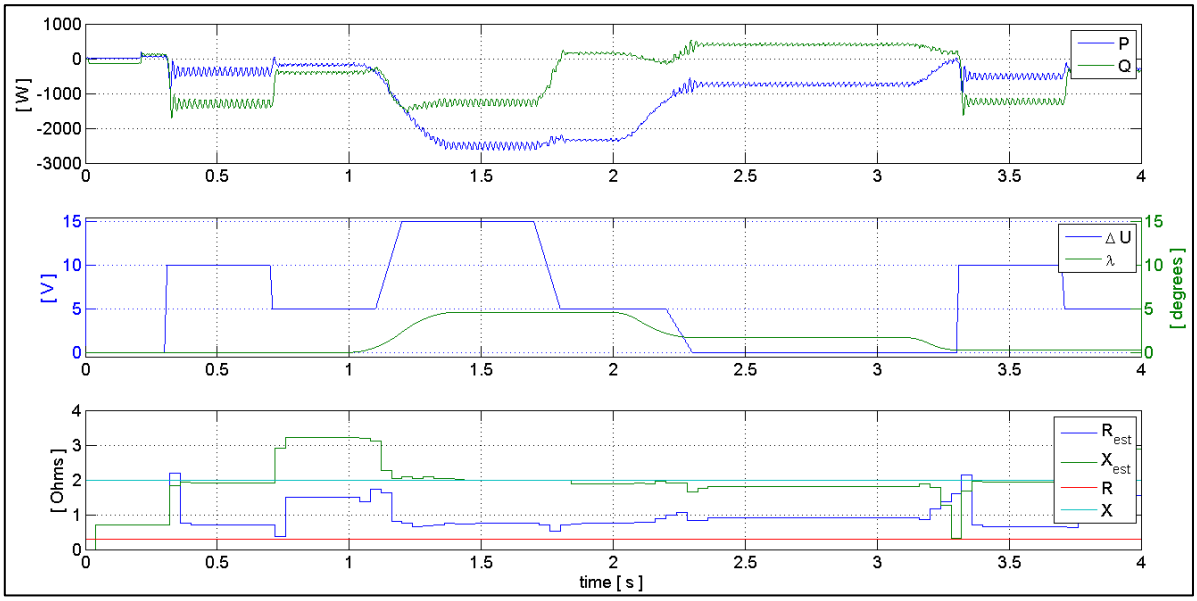


Figure 5-49: Impedance Estimation Performance for a Grid-tied Inverter with Higher Power Flow

However, the previous figures show that the estimated resistance and inductance are less accurate when the controlled voltage source is a passively filtered power inverter compared to those obtained with the ideal controlled source. This might be caused by the intrinsic characteristics of the inverter and not by the RLC passive filter because, once the inverter is replaced by the ideal voltage sources but with the RLC filter as shown in Figure 5-50, the estimation is more precise and converges to the expected values (Figure 5-51).

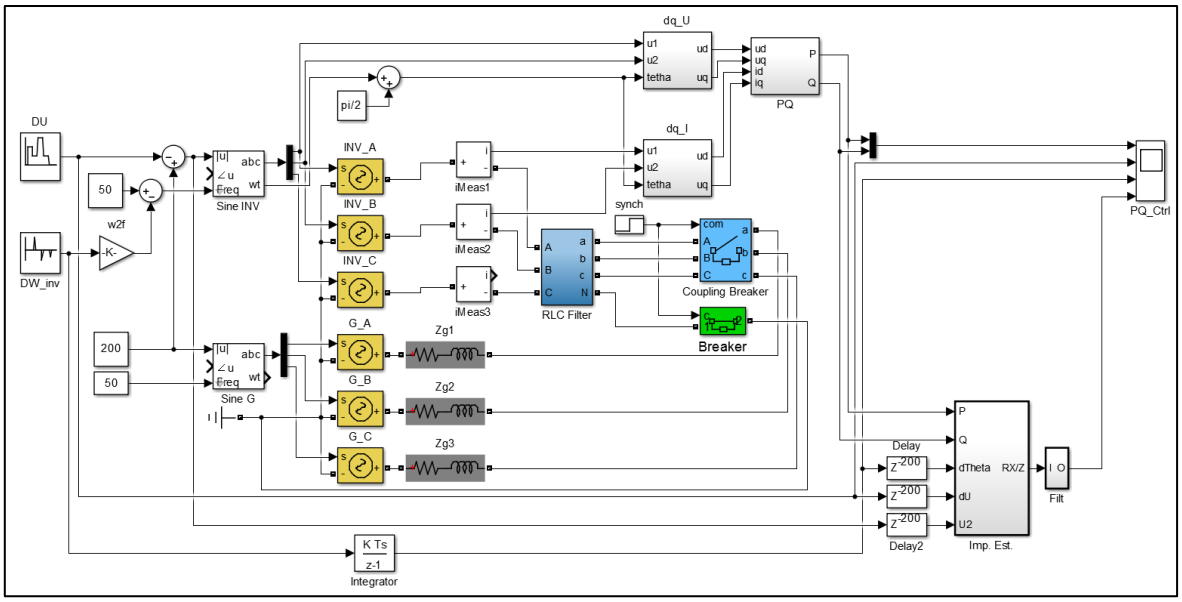


Figure 5-50: Simulink – Impedance Estimator Block Diagram for a Passively Filtered Ideal Source Coupled with another Ideal Voltage Source

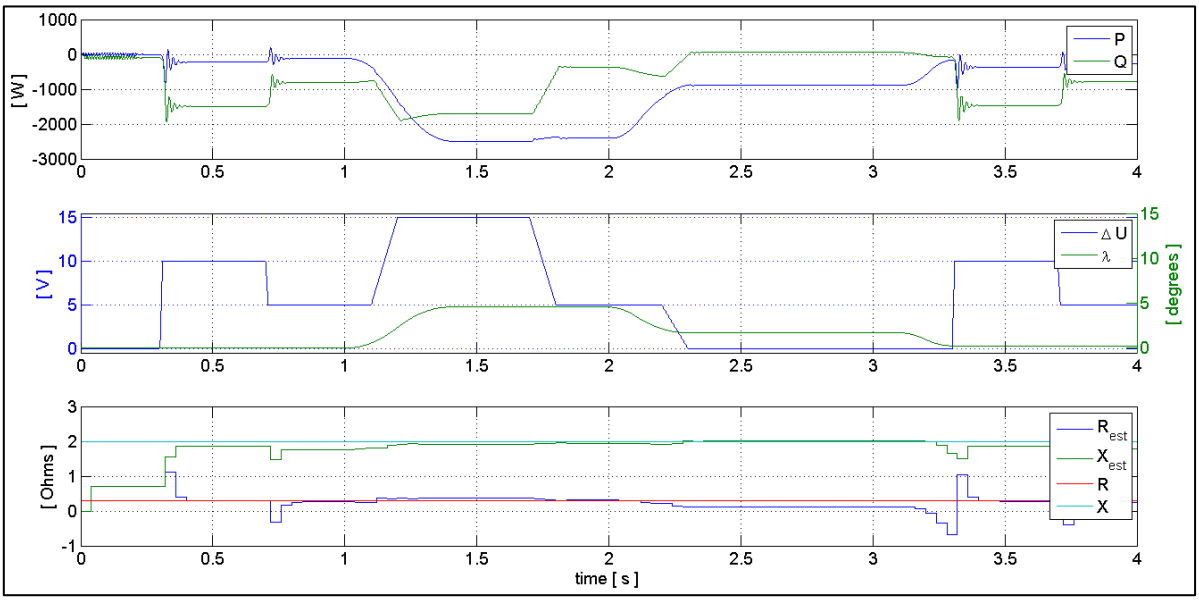


Figure 5-51: Impedance Estimation Performance for a Passively Filtered Ideal Source Coupled with another Ideal Voltage Source

Based on all the above-mentioned behaviour of the estimator model, it is then recommended to use it for systems with low dynamics. In order to avoid transient disturbances, a numeric filter can be implemented to reduce the estimation error level during the transient phases. It is also better to work with low oscillating input values. Mainly the active and reactive power should be as steady as possible. They can also be numerically filtered if they are oscillating. In the case of the grid-tied inverter, the power oscillations are caused by the unbalanced currents. In such a case, finding the reason and correcting the current asymmetry will solve the problem of power oscillation rather than simply numerically filtering. Another important point is the estimator sampling frequency. It should not be faster than the system time constant including that of all measurement equipment and also all the numerical elements like filters. These time delays should be taken into account in order to improve the estimation,

i.e. the active and reactive power, the phase angle difference, the voltage magnitude difference and the inverter applied voltage.

Impedance estimator in real conditions

In the previous configuration and results, the main power grid to which the controlled voltage source is coupled is fully stable and neither its frequency nor its voltage magnitude changes over the time. In real conditions, this is not the case. Due to a load variation, the frequency and the voltage magnitude of the grid change. This means that the simple integration of the controlled frequency variation is not a reliable method for determining the phase angle difference between the grid and the controlled voltage source. A good measurement point of any grid state variation (frequency or magnitude) is the PCC especially in cases where the grid impedance is considerably lower than that of the coupled voltage source (see section 5.5.1). The phase difference between both voltage sources is approximated to the measured phase angle difference between the controlled voltage source (inverter) and the voltage at the PCC λ'. Likewise, the magnitude difference is approximated to the difference between the PCC voltage magnitude and that of the inverter's voltage $\Delta U'$. Therefore, biased but still representative value of the system conductance and reactance are defined as

$$\begin{bmatrix} G' \\ B' \end{bmatrix} = \frac{2}{\widehat{U}_2} \cdot \frac{1}{(\Delta U')^2 + (\lambda' \widehat{U}_2)^2} \begin{bmatrix} -\Delta U' & \widehat{U}_2 \lambda' \\ \widehat{U}_2 \lambda' & \Delta U' \end{bmatrix} \begin{bmatrix} P \\ Q \end{bmatrix} \qquad (5\text{-}27)$$

The Figure 5-52 depicts how the PCC voltage properties are used by the impedance estimator. Its phase angle difference to that of the inverter is derived from its direct voltage component in the inverter frame. This last value is then divided by its magnitude and negated.

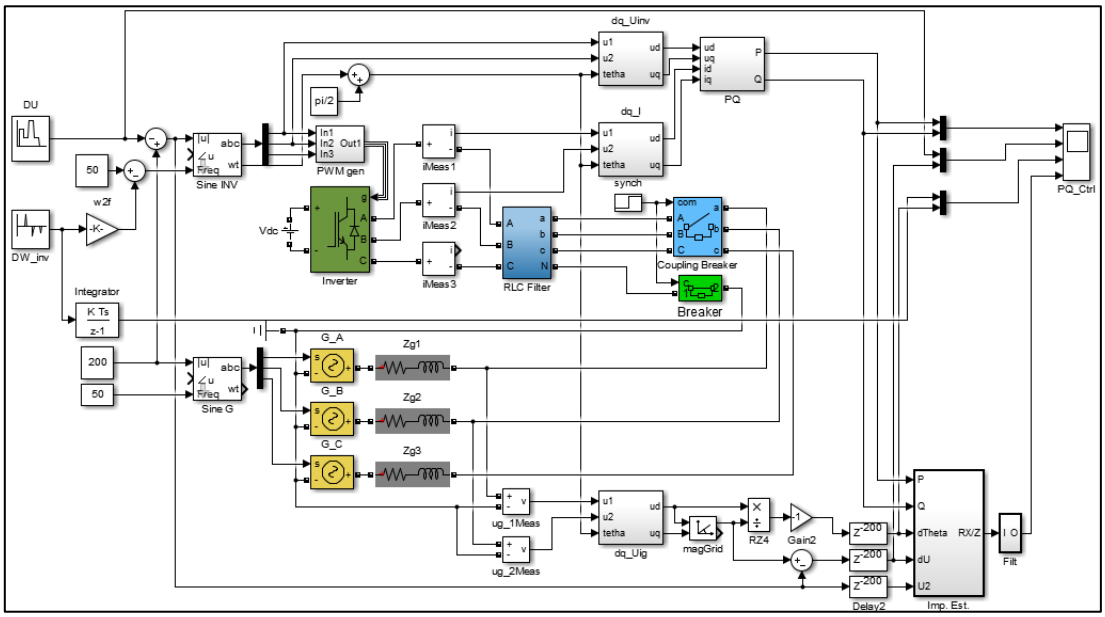


Figure 5-52: Simulink Block Diagram - Impedance Estimator Using PCC´s Voltage Magnitude and Phase-shit

The results of the estimation using the PCC voltage properties are shown in Figure 5-53. It can be noticed that the real control variables (magnitude difference and phase shift) differ as expected from those measured at the PCC. However, the measured values represent a very good indicator of any system change. Depending on the interaction of both voltage source impedances, a magnitude variation on one source has an impact on the PCC voltage or phase angle or even on both characteristics. Concerning the impedance estimation, the provided

values are not necessarily the expected ones since the input variables are wrong. It is interesting to point out that the estimated resistance and inductance strongly varies with the exchanged active and reactive power. Further investigations are required to fully understand the meaning of the calculated values. Even though they are really different from the expected resistance and inductance values, the following paragraph shows how meaningful they are, since the power control based on these values works perfectly.

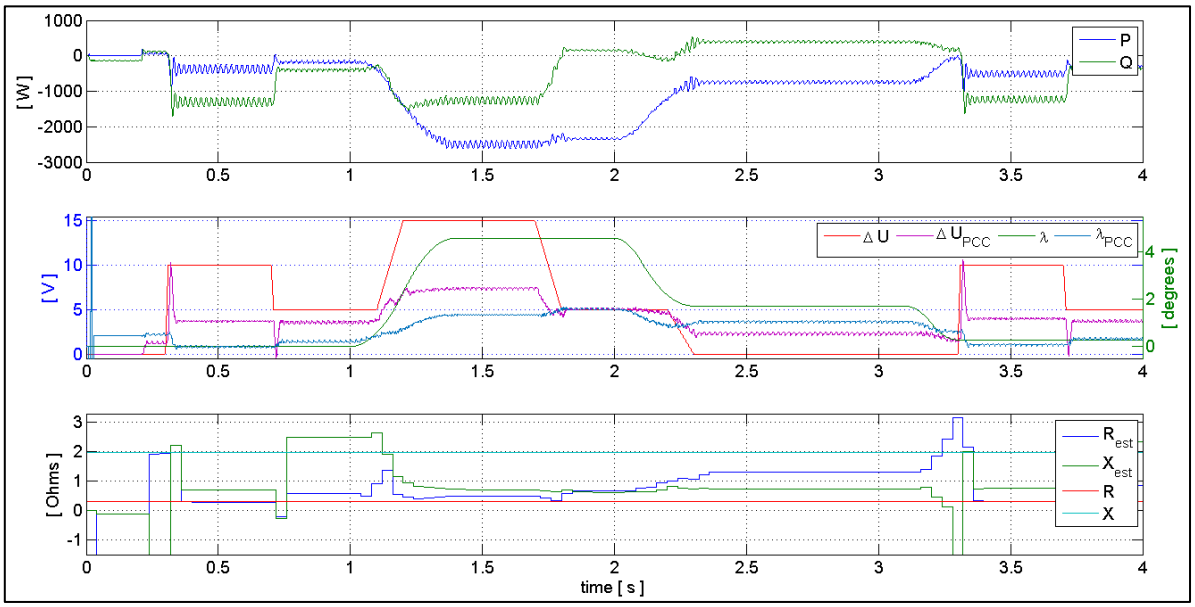


Figure 5-53: Impedance Estimation Using PCC Voltage Magnitude and Phase-shit

5.5.5.2 Power Control Loop

In order to get the impedance estimator to work properly, the actual phase angle difference between the grid voltage and the controlled voltage needs to be well known. This constraint plays a big role in the choice of the synchronisation method. The PLL-based synchronisation works well but becomes useless once the two voltage sources are coupled because their previously different measurement points are now the same. This means that the power control system requires another reference point in order to determine the amplitude and phase difference, therefore, another logical algorithm has to be implemented for that purpose. The first attempt is to consider a zero phase difference at the coupling time. Then the frequency variation imposed by the power regulation is simply integrated over the time and it is supposed to reflect the phase difference. However, there is no confidence that the applied phase variation is effectively the real phase difference between the grid and the filtered inverter voltages. In his work in [93], Markus Jostock has shown, as depicted in *Figure 5-54*, that the frequency at the PCC between both voltage sources, differs from the frequency of the two connected sources. When the frequencies are slightly different, the measured frequency is much closer to the arithmetic average of both frequencies. This means that the simple integration of the frequency variation imposed by the power regulation does not reflect the real phase angle between the voltages. Another disadvantage of this method is that the phase can also change if (and it is regularly the case) the grid frequency varies. In this case, only the sudden and unexpected variation of the exchanged power will be the only one indicator of a momentary phase shift between both voltage sources.

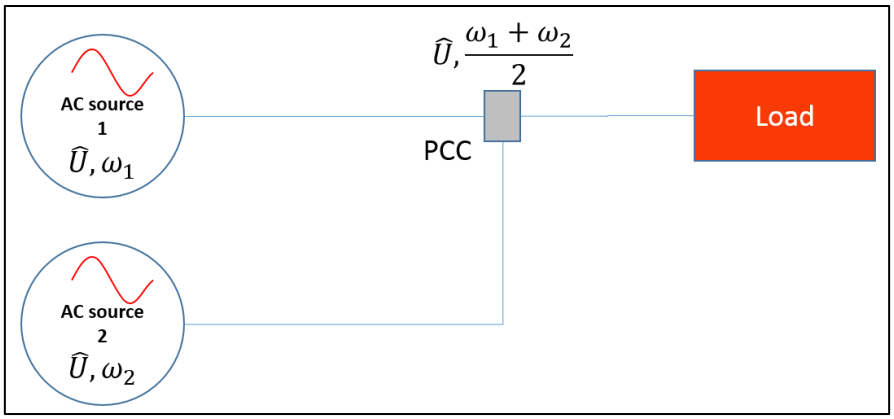


Figure 5-54: Average Voltage Magnitude and Frequency at the Point of Common Coupling

In contrast, a phase shift control of both voltages sources realised in the inverter frame offers information that is more useful. The voltage direct component gives a direct information about the phase shift between the reference frame (that of the inverter) and the filtered voltages. This value can be directly used for the power control loop. Furthermore, this value reflects not only the phase shift variation caused by the power regulation but also any phase deviation that has been eventually caused by a variation in the grid, notably the frequency variation (assuming that a phase jump is almost impossible for the grid except in the case of a network fault). This is the main reason why this last method of phase shift control is preferred and is then used for the power control.

The working principle of the power control is presented in Figure 5-55. It is actually a simplified system that does not integrate the synchronisation process. Therefore, the two voltage sources are supposed to have been already successfully coupled.

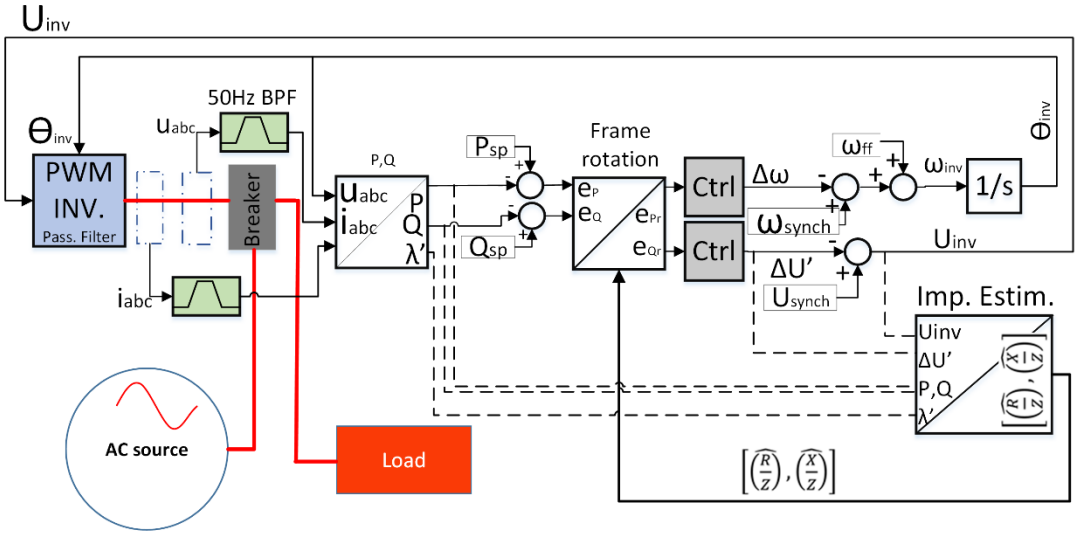


Figure 5-55: Grid-tied Power Control Loop Including the Impedance Estimator

First, the voltage and current are measured at the point of common coupling and filtered to extract only the 50 Hz component since only the control of the fundamental frequency is of interest. The active power and the reactive power are computed based on the filtered values. The phase shift between the inverter reference frame and the measured voltage is determined through the computation of the direct voltage component in the inverter frame. Dividing this value by the voltage amplitude gives the actual phase shift λ. In fact, the value obtained after the division is normally the sinus of the phase difference. Because this value is

relatively small, its sinus can be approximated to itself. The impedance estimation block "Imp. Estim" uses the power component values P & Q, the magnitude difference ΔU as well as the inverter voltage magnitude U_{inv} and finally the actual phase shift λ, to estimate the impedance components R & X. The estimated impedance components allow the transformation of the actual and the set-point powers into a rotated impedance frame (block "Imp. Frame rotation", in order to practically decouple the P and Q control. After that rotation, the obtained virtual reactive and active powers P_r & Q_r are generated independently from each other. On the one hand, the rotated reactive power error e_p is then regulated to zero through a controller, which, for a very short time, modifies the inverter frequency that will have a direct impact on the phase shift between the grid and the inverter voltages. On the other hand, the rotated active power error e_q is regulated to zero by controlling the voltage magnitude difference. This newly computed magnitude difference is then subtracted from the inverter magnitude U_{synch} calculated for the synchronisation.

5.5.5.3 Simulation Configuration

The Simulink model (Figure 5-56) used to illustrate the grid-tied inverter power control has the following characteristics:

- A three-phase 400 V line voltage of the power grid composed of an ideal voltage source and a given impedance for each phase. The impedance Zg is defined by the connected resistance Rg and inductance Lg.
- The controlled VSI is fed by a constant 600V DC source. The PWM is based on the intersection method. The triangle wave has a frequency of 15 kHz.
- The coupling circuit breaker is set to connect both voltage sources after 0.2 sec. They are configured to be synchronized right from the beginning. This breaker represents de PCC where the voltage is monitored and decomposed into its direct and quadrature component inside the inverter frame in order to extract its phase shift and magnitude.
- The delivered inverter power is calculated using the PCC voltage and the current flowing out from the RLC filter since the focus point is the power injected into or drawn from the grid. The RLC filter has the resistance R_{filter}, and inductance L_{filter} and both are connected in parallel with the capacitance C_{filter}.
- FIR filters with 401 taps are used to extract the 50 Hz components in the measured voltages and currents. They have a sampling frequency of 20 kHz. The impedance estimator is much slower compared to the voltage and current acquisition process. It has a frequency of 25 Hz.
- The magnitude difference, i.e. the virtual (rotated) active power controller is a PI controller with the parameter K_{pu} and K_{iu}. The controller of the phase angle difference, i.e. the virtual (rotated) reactive power also has a sampling frequency of 40 Hz. It is a simple proportional controller with the coefficient K_{pa}. In fact, the controller briefly changes the frequency of the inverter and then is set back to zero after the inverter has created the desired angle.
- In order to better match the reality, the impedance estimator has been modified by delivering the absolute value of the computed estimations since neither a resistance nor an inductance can be negative. Working with absolute values is essential for the control because the estimation and the control model are based on values supposed

to be always positive or equal to zero. Also for a properly running control strategy, the estimated values are filtered using a weighted moving average filter.

- The coupling occurs at the time 0.2 sec and the power flow control 100ms later, i.e., at the time 0.3 sec.

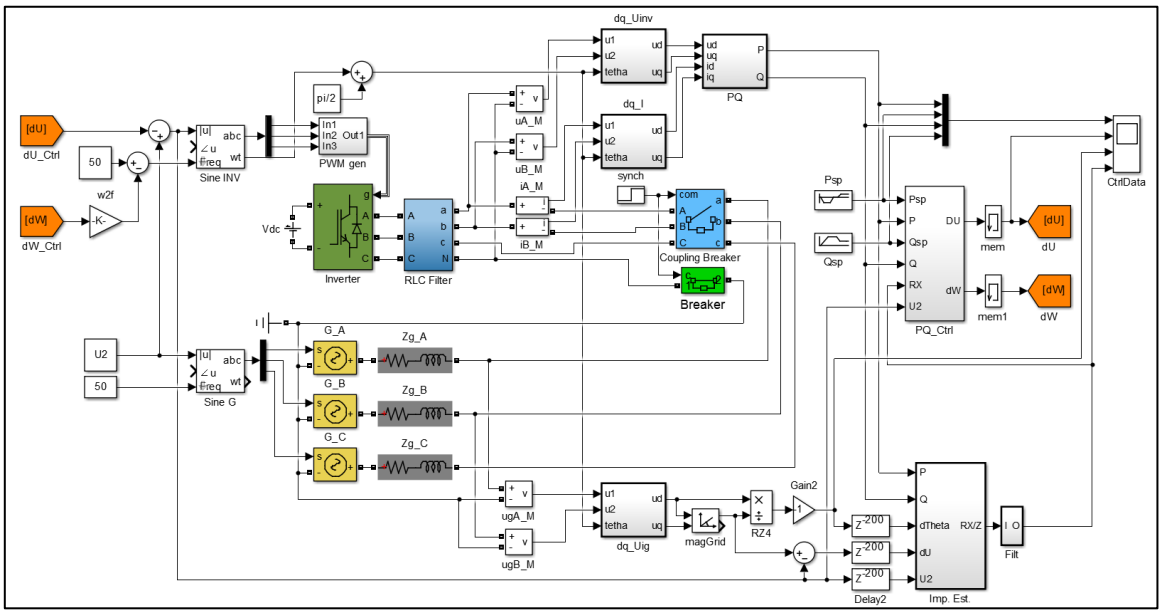


Figure 5-56: Simulink Block Diagram - Basic Grid-tied Inverter Control Diagram

5.5.5.4 Simulation Results

The Table 5-6 presents the values of the inverter passive RLC filter and the power controllers. These values are fixed and remain unchanged for all the simulated scenarios.

Table 5-6: Relevant data of the inverter passive RLC filter and of the power controllers

R_{filter}	L_{filter}	C_{filter}	K_{pu}	K_{iu}	K_{pa}
0.2Ω	1.56mH	7µF	$4*10^{-4}$p.u	5 p.u	$4*10^{-2}$ p.u

Each following scenario describes a particular state of the system where the same estimation and regulation principles are applied to achieve the power control.

Scenario 1 – Inverted coupled to a stable unloaded grid

The direct interaction between the VSI and the power grid is investigated in this scenario. The power generated by one source is, except the losses, completely absorbed by the second one. The grid's resistance R_g is 0.2Ω and its inductance L_g three times that of the filter, i.e. 4,7mH. The results of the inverter power control are depicted in Figure 5-57. The active and reactive power follow the set points with a good precision and timing except at the beginning of the control process. This is caused by the impedance estimator that delivers inaccurate values at the beginning and these estimated values are also filtered, this increases the time until the valid values are reached. As expected, the estimated impedance components do not remain constant over the time. The values change with the exchanged active and reactive power.

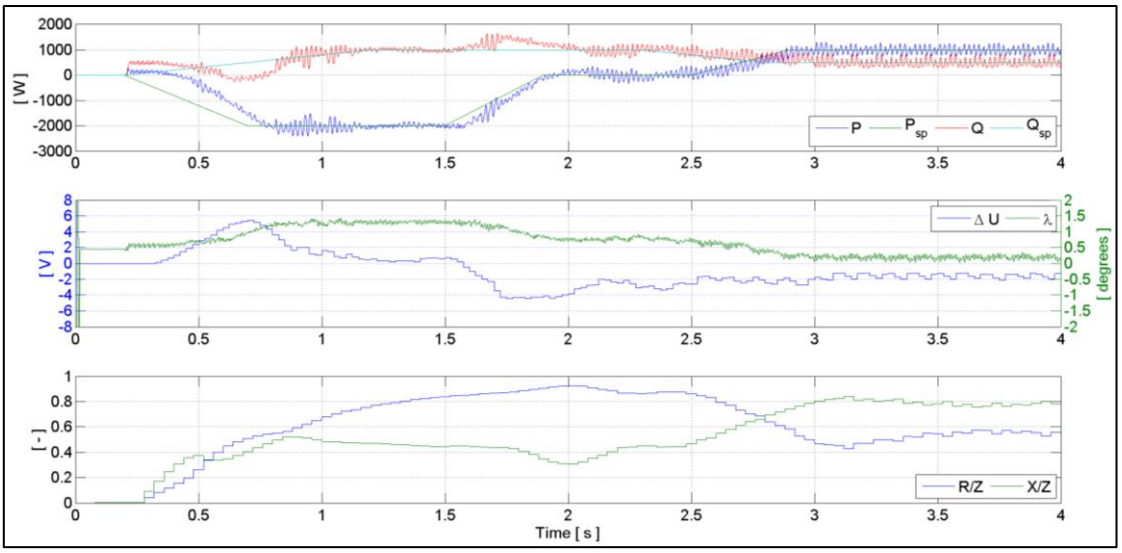


Figure 5-57: Inverter Power Control with Unloaded Grid

Scenario 2 – Inverter coupled to a stable grid feeding a pure resistive and stepwise varying load.

The resistive load profile is depicted in Figure 5-58. The first 1000 W load starts at time 1 sec and stops 2 seconds later. The second load, with the same power, is connected from the 2nd to the 3rd second.

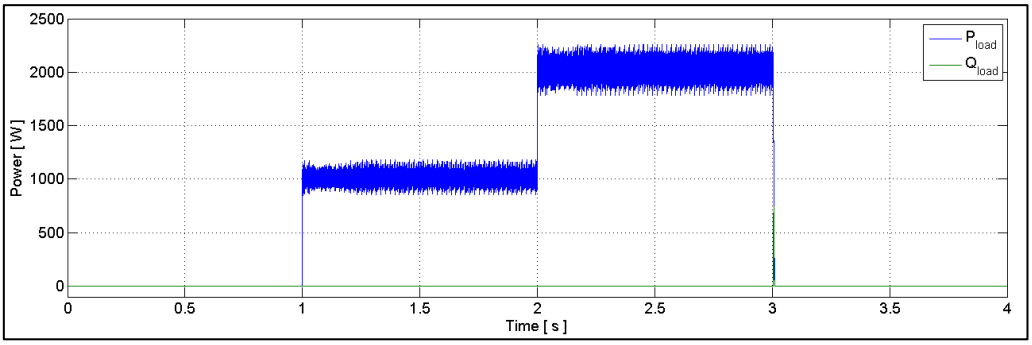


Figure 5-58: Resistive Load Profile

The following Figure 5-59 shows how the inverter power control reacts to the system states variation induced by the sudden connection and disconnection of the resistive loads. In the same time, the active and reactive set points remain constant for a better observation of the control behaviour. In this case, the P.Q controls remain stable too. On the active power curve only is visible how switching on and off the load impacts the control. A brief power peak appears and it is subsequently recovered by the controllers in less than 250 msec. The impedance estimator is not significantly impacted by the load profile. The estimated values show a little fluctuation caused by the sudden power change but go back to the previous values as the active and reactive power are stable. The power control variables ΔU and λ indicate that the active power is controlled by the phase shift λ. This corroborates the well-known control strategy for inductive power grid where the active power is controlled by the phase angle difference and the reactive power by the voltage magnitude difference. This occurs here since the resistive load switched on reduced the whole resistance of the system, so the inductive part of the whole impedance gets higher.

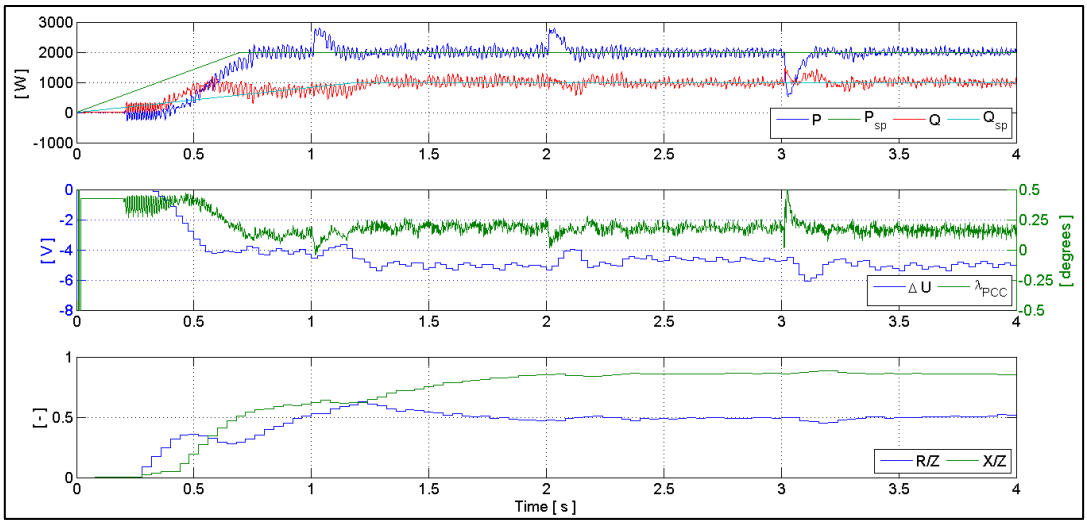


Figure 5-59: Inverter Power Control with Stepwise Varying Resistive Load

Scenario 3 – Inverter used as a power factor controller for the main power grid.

This test demonstrates the behaviour of the power control dealing with not only a resistive load but also inductive or capacitive load. The goal here is to use the power inverter to deliver a constant active power and at the same time be fully responsible for the reactive power required by the load. This means that the main power grid is delivering only the remaining active power leading to a power factor of 1 from the main grid point of view. Similarly, to the previous test, the connected load is changing over the time. The inverter reactive power set point is set to the measured reactive power of the load. The results are shown in Figure 5-60 that depicts the power flow among the three main part of the system, i.e., the inverter, the grid and the load. The active, as well as reactive powers required by the load, are depicted on the graph at the bottom. In order to keep a power factor of 1 for the grid, all the reactive power should be generated by the inverter leading to a zero reactive power by the grid. The Figure 5-76shows that the inverter successfully fulfils the expectations. The graph on top indicates that the inverter delivers the exact reactive power required by the load while the grid remains unaffected (except during the transient phases). Concerning the active power, it can be observed that the total active power delivered by the inverter is shared between the grid and the load. Before the load is connected (from 0 to 1 sec), all the active power is injected into the grid. Once connected, the load requires only half of the inverter power production so the remaining half continues to be fed into the grid. The second load is then connected and the required power doubles matching the actual inverter delivered power. So the active power of the grid falls to zero as all the inverter active power is used to feed the load. When the entire load is suddenly disconnected, the reactive power not being required is regulated to zero while all the active power from the inverter is diverted to the grid.

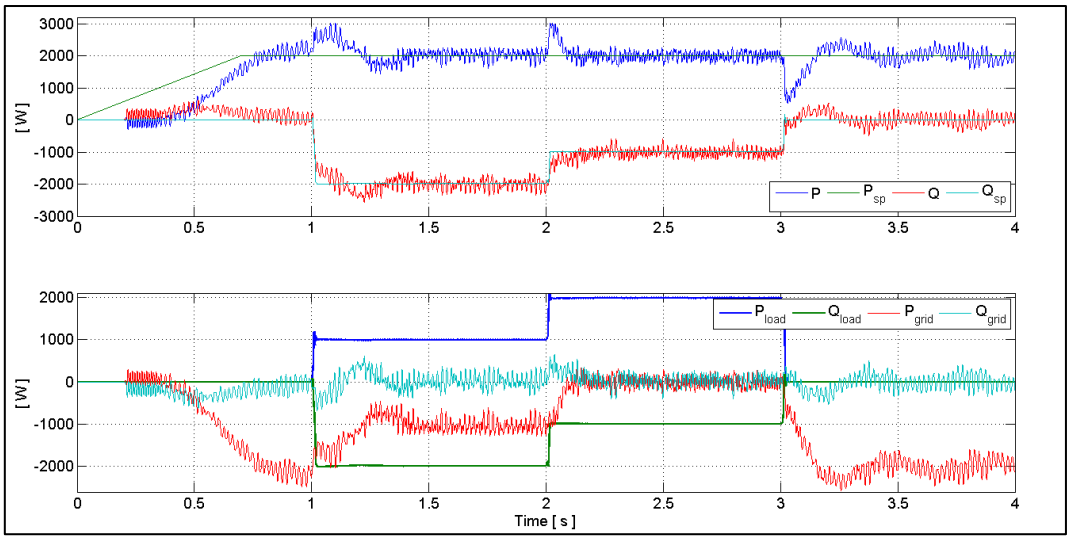


Figure 5-60: Inverter Power Control as a Grid Power Factor Controller

5.5.6 Power Inverter as Voltage Harmonic Compensator

In order to be used as a grid-tied unit for the harmonics compensation, the APF has more constraints to respect than in the case it is used in the off-grid operation. The harmonic compensation algorithm itself remains unchanged but the fundamental frequency control has more steps to achieve. First, the fundamental voltage has to synchronize to the grid voltage, then the output of the power unit has to be coupled to the grid and finally, in order to avoid undesired power transfer between the two connected power sources, a power regulation to zero has to be performed. Once these steps are achieved then the harmonic compensation can be started. The following chapters give the details of these different steps and the final objective performance, which is the harmonic compensation, is analysed.

5.5.6.1 Grid-tied Harmonic Compensation at Nominal Frequency

The Figure 5-61 depicts the results of the harmonics compensation in a grid-tied situation. After the synchronization and the coupling occurring at the time 0.362 sec, a 10 kW resistive and non-linear load (identical to the load in the previous chapters) is connected at the time 0.6 sec. This means that the synchronization is realized on a non-distorted grid voltage. The first harmonic compensation (of the 5^{th} harmonic) starts at 0.8 sec and the other compensations start one after the other with a delay of 0.2 sec. The harmonic compensation process is exactly the same as in the off-grid situation. The PLLs and magnitude controllers' configuration, as well as the FIR filters, are unchanged. After the synchronization has occurred, the level of the voltage magnitudes increases slightly because of the imperfect sinusoidal voltage delivered by the inverter. The voltage magnitudes are still quite low but high enough to increase the THD from zero (perfect sinusoidal grid voltage) up to 4%. Once the load is connected, the harmonic level induced by the non-linear load is much higher. The THD rises to about 13%. 0.2 sec after the harmonics compensations are applied and the THD has improved as the harmonics magnitudes are lowered. Thus the harmonic compensation works properly also in grid-tied conditions. The only step to perform before applying the compensation is the synchronization. The previously described compensation has been done for an exact 50Hz grid frequency. The focus is set now to the dynamic behaviour of the harmonics compensation when the grid frequency varies from the nominal frequency and also in the case for sudden non-linear load change.

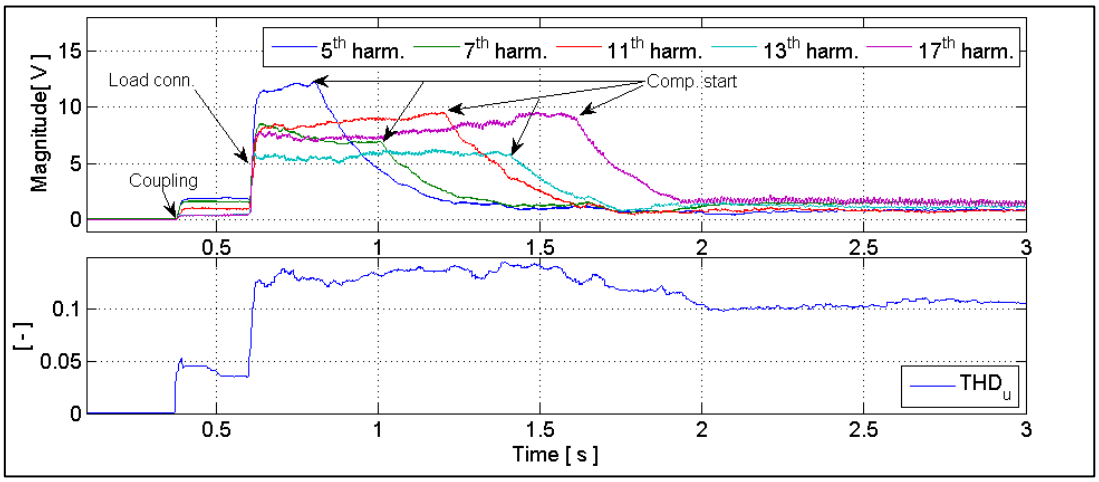


Figure 5-61: Harmonics Magnitudes Control and Grid Voltage THD

5.5.6.2 Harmonics Compensation by Nonlinear Load Change at Nominal Frequency

The Figure 5-62 shows how the compensation works even when the level of harmonic changes dramatically. In the simulation, the non-linear load is switched off after 3 seconds. The level of detected harmonic jumps and these are nothing but the compensation voltages. These will then be progressively regulated to zero. A too fast (dynamic) compensation algorithm (PLL and amplitude regulator) could lead to an indefinite increase of the harmonics after the non-linear load is switched off, because the system will attempt to instantly mitigate the detected harmonics but these last are its own generation, leading to a never-ending self-excitation.

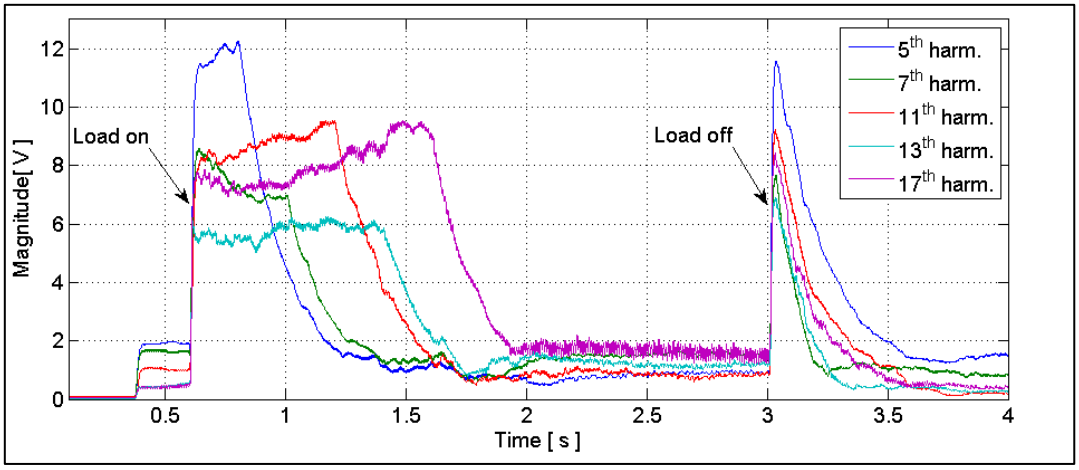


Figure 5-62: Harmonics Magnitudes Control by Sudden Load Change at Nominal Frequency

5.5.6.3 Harmonic Compensation at the Maximum Grid Frequency (50.5 Hz)

In the scenario whose compensation results are depicted in Figure 5-63, the frequency of the grid on which the inverter is coupled has been changed from 50 to 50.5 Hz.

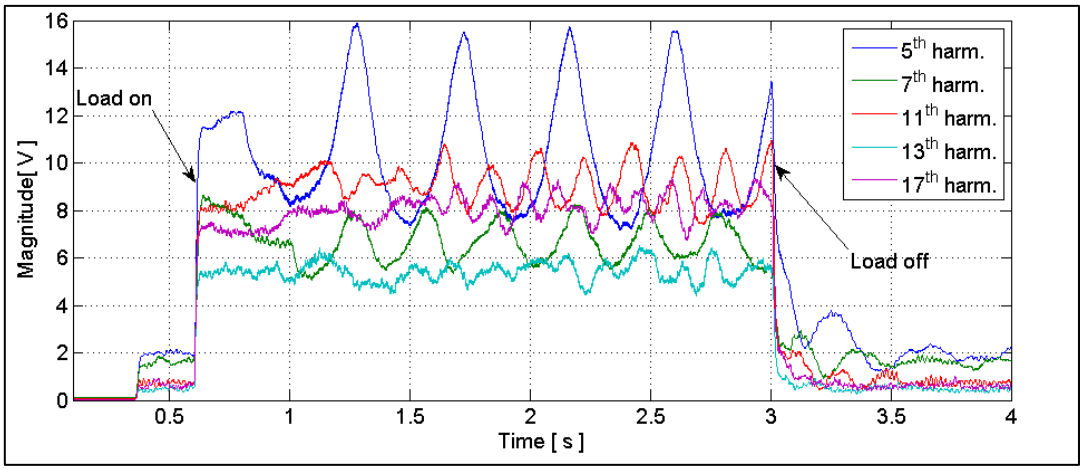


Figure 5-63: Harmonics Magnitudes Default Control at Maximum Grid Frequency

The compensation algorithm, with the same configuration (PLL and PI amplitude regulators), does not work as expected. A look at the delivered values of the PLL for the 5th harmonic (Figure 5-63) shows that the PLL parameters are not optimised for this frequency. The compensation being totally dependent on the PLL computed values, cannot work in this case.

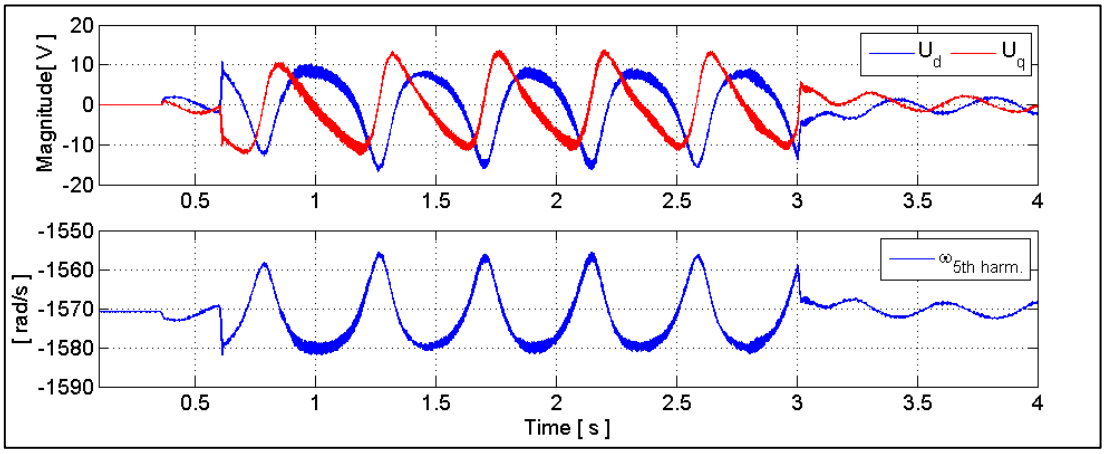


Figure 5-64: 5th Harmonic Tracking PLL's Values at Max Frequency

An optimisation of each harmonic PLL and amplitude compensators has been performed and summarised in Table 5-7. The values of the PLLs and of the magnitude controllers work very well for the nominal frequency. Nevertheless, the new values offer an acceptable behaviour of the compensation when the frequency is increased to 50.5 Hz.

Table 5-7: Parameters Values for the PLLs and the Amplitude Controllers

		Nominal frequency (50Hz)				Grid frequency 50.5 Hz			
5th harm.	PLL	k_p	1	k_i	2	k_p	2	k_i	12
	Amp. Comp.		.1		8		.1		4
7th harm.	PLL		1		2		2		20
	Amp. Comp.		.1		8		.1		4
11th harm.	PLL		1		2		3		24
	Amp. Comp.		.1		8		.1		4
13th harm.	PLL		1		2		5		50
	Amp. Comp.		.1		8		.1		4
17th harm.	PLL		1		2		8		24
	Amp. Comp.		.1		8		.1		4

The result depicted in Figure 5-65 shows that the harmonic compensation system works also after a sudden load change. Each harmonic compensation algorithm needs a fine-tuning that is not straightforward but hard to find.

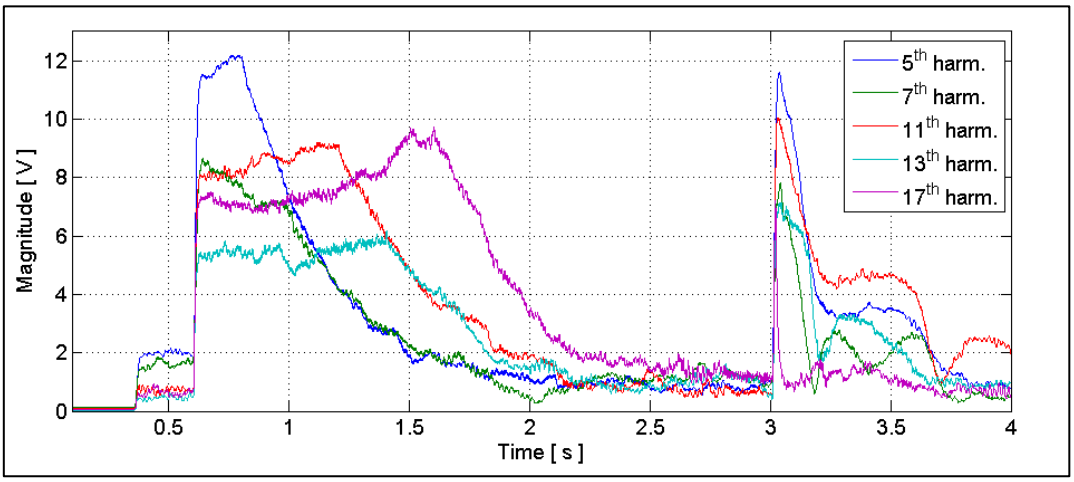


Figure 5-65: Harmonics Magnitudes Adapted Control at Maximum Grid Frequency

A second correction performed to improve the stability of the PLL is to start the compensation only when the PLL is close to its steady state. In this example, this limit is set by setting a maximum value for U_d ($U_{d,max} = 5\ V$), so that the magnitude regulation should start when the absolute value of the computed U_d value is below that limit. A direct regulation right after the occurrence of the harmonics has a feedback that strongly affects the PLL. Then the wrong computed value of the PLL causes the regulation to be also wrong. This problem occurred mostly for the harmonics of higher frequencies (13th and 17th). An alternative to this solution is to reduce the parameters of the magnitude PI controllers to make them less dynamic.

Another aspect that may affect the harmonics control is the FIR filters that deliver a 180° phase shift with zero attenuation only at the nominal frequency. In fact, a different attenuation may not represent a big concern because the magnitude controllers adapt their output value so that the measured remaining magnitude drops down to zero. The most sensible part is the phase shift that cannot be recovered by the regulation. This aspect has not been corrected in the previous simulation but somehow, the regulation still successfully manages to mitigate the harmonics.

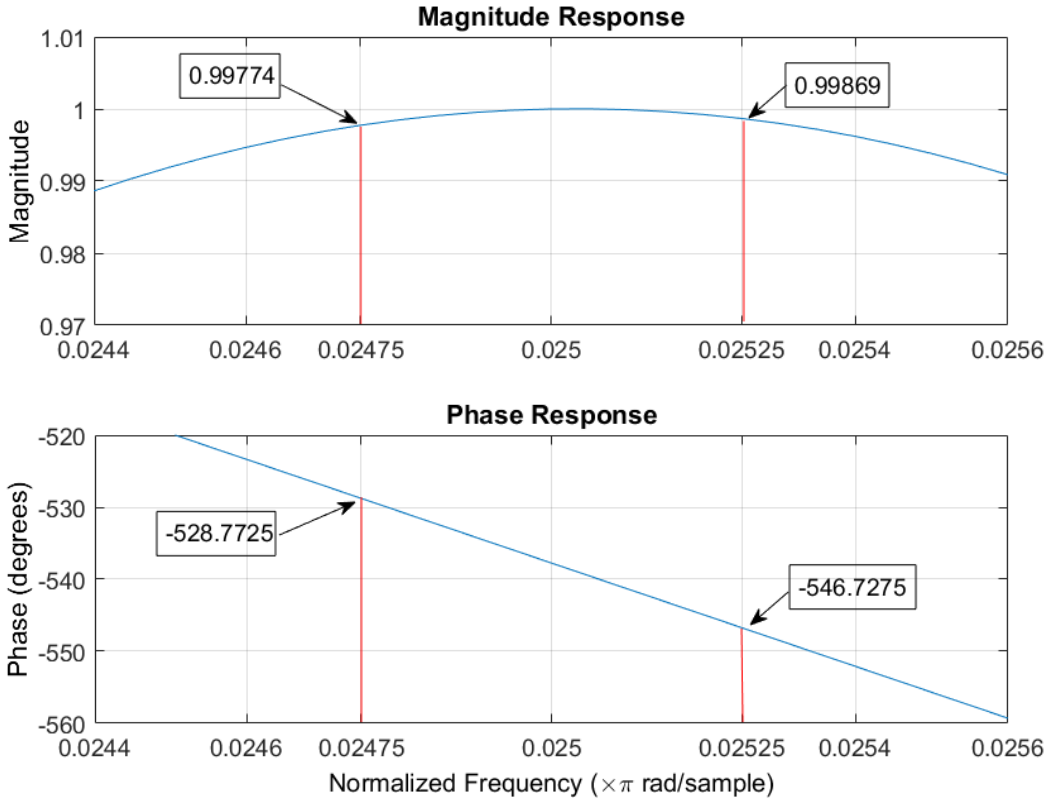


Figure 5-66: Magnitude and Phase Response for the 250 Hz FIR Filter with 401 Taps

The Figure 5-66 shows the magnitude and phase response of the 250Hz FIR filter. The points marked on the plots are referring to the normalized minimum, nominal and maximum frequency our system can reach ($50\text{Hz} + -1\%$) this means for the 5th harmonic (50Hz +-1%) x5. For example, if the system is running at its highest frequency, the attenuation slightly increases but remains absolutely acceptable and the output magnitude is still 99.8% of the input amplitude. Concerning the phase shift, it will go from -540° ($-180°\text{x}5$) to approximately -549° ($-180° - 9°$). This means the FIR filter generates a phase shift of 9° between the input and the output signal.

With the help of the filter analysis tool of MATLAB, fvtool, the following Table 5-8 has been established and it summarizes the different phase shifts caused by each FIR filter.

Table 5-8: FIR Filters Phase-shift max and min Errors Caused by Input Frequency max and min Variation

Freq. [Hz]	Norm. freq. [π rad/ sample]	Phase shift [degrees]	Norm. min freq. [π rad/ sample]	Phase shift [degrees]	Phase diff.	Norm. max freq. [π rad/ sample]	Phase shift [degrees]	Phase diff. [degrees]
50	0,005	-179,55	0,00495	-177,7545	-1,7955	0,00505	-181,3455	1,7955
250	0,025	-537,75	0,02475	-528,7725	-8,9775	0,02525	-546,7275	8,9775
350	0,035	-536,85	0,03465	-524,2815	-12,5685	0,03535	-549,4185	12,5685
550	0,055	-175,05	0,05445	-155,2995	-19,7505	0,05555	-193,005	17,955
650	0,065	-174,15	0,06435	-150,8085	-23,3415	0,06565	-197,4915	23,3415
850	0,085	-532,35	0,08415	-501,8265	-30,5235	0,08585	-562,8735	30,5235

It can be noticed:

- All the actual phase shifts at nominal frequencies differ from the expected theoretical value of -180° for every designed FIR filters.

- The higher the frequency the higher the phase shift error at nominal frequency. The phase shift error obtained for a given harmonic (at his highest or lowest frequency value) is equal to the harmonic order times the error of its fundamental frequency. This can be explained by the fact that the number of coefficients, as well as the sampling frequency, is the same for all the targeted frequencies. This causes the filter of a higher frequency to be less accurate (inversely proportional to the harmonics order) than those of a lower frequency.
- The variation rate (linear) of the difference between the phase shift at the nominal frequency and that at a different frequency increases with the nominal frequency. For the same frequency variation, for example +1%, the phase shift variation is 1,79° for the 50Hz FIR filter whereas the 17^{th} harmonic (850Hz) FIR filter presents a variation of +30.5°.

Based on these observations, a correction of the phase shift should be performed since not only the expected phase shift is not respected but also because the phase shift deviation when the frequency differs from the nominal frequency, is not negligible. Another approach to solving this problem would be to design each filter differently so that they all have a phase delay very close to -180° at their nominal frequency and the phase delay should not deviate too much when the filtered frequency varies (within the variation limits). This can be done (but still needs to be verified) by defining a different sampling frequency and different coefficient numbers for each FIR filter. A good compromise should be found between the phase shift deviation and the magnitude attenuation when the signal frequency changed from the filter's rated frequency. For FIR filters, a great number of coefficients leads to a narrower passband but steeper phase shift.

5.5.6.4 Harmonics Compensation Based on the Inverter Reference Frame

This technic is very similar to the synchronisation process based on the inverter reference frame (phase angle) presented in 5.5.2.2. Since every harmonics frequency is a multiple of the fundamental frequency, knowing the inverter fundamental reference frame and frequency means that all the corresponding harmonics frequency and also frames are known. Then, each harmonic phase angle is deduced by multiplying the inverter phase angle by the order of the harmonic taking into account the direction of rotation of the harmonics. This means that the 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th} phase angles are obtained by multiplying the inverter fundamental phase angle by -5, 7, -11, 13 and -17 respectively. This method is illustrated in Figure 5-67. Unlike the PLL-based voltage control (see Figure 5-2), this system relies on the internal VSI frame that allows the reduction of the control time through the suppression of the PLLs frame (phase angle) calculations.

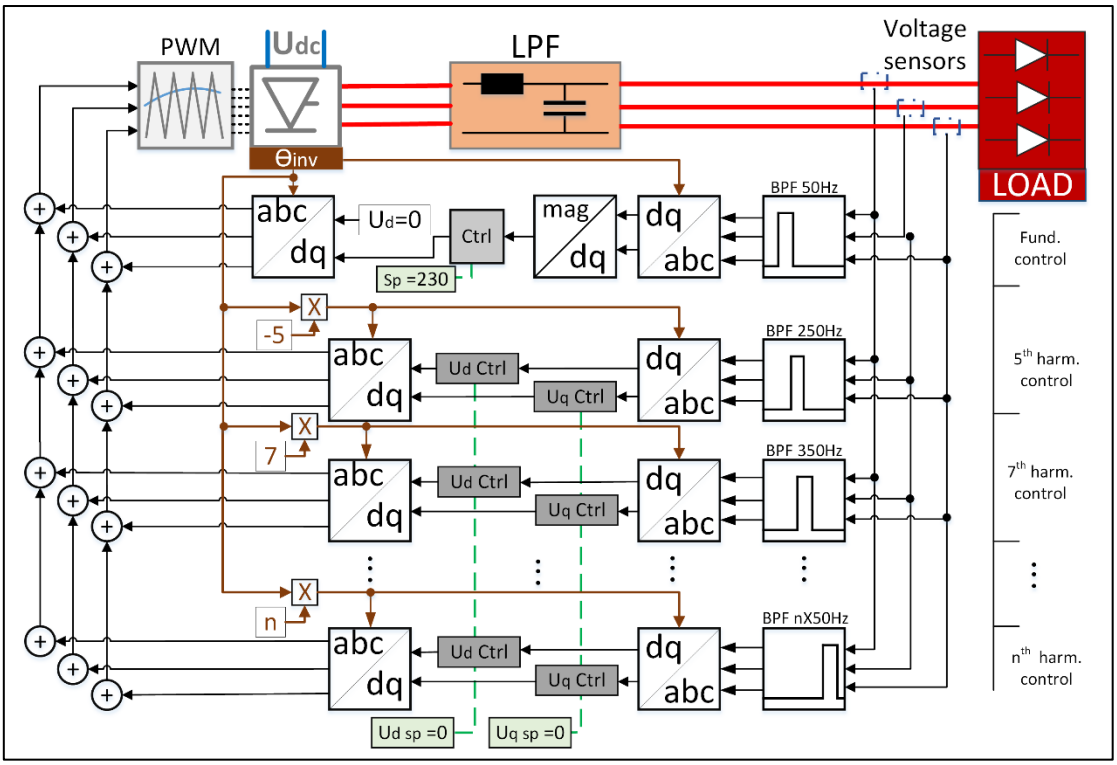


Figure 5-67: Closed Loop Diagram of the Selective Harmonic Compensation Based on the Inverter Frame

The previous detailed harmonics compensation method based on PLLs has depicted some stability issue due to the fact that each harmonics detection and compensation frame is totally dependent on a single subsystem that might not be as robust as wanted in every grid state. Basing every calculation on the inverter frame copes very easily with this issue in terms of stability because this frame remains stable, might deviate of +- 1% as long as the inverter works. Furthermore, the computational load for the harmonics control is substantially reduced since the PI controllers required for each harmonic PLL is no longer needed.

The following figures depict the full stability of this compensation method especially when the system frequency is different from the nominal 50 Hz frequency. The simulated scenario is the same as that used for the PLL-based compensation. The inverter is synchronized to the power grid, the load is connected at time 0.6 sec and at 0.8 sec the harmonics compensations start one after the other from the 5^{th} harmonic to the 17^{th} with a 0.2 sec time delay. The load is disconnected at time 3 sec as the harmonics compensation continues. Figure 5-68 shows the harmonics magnitude control achieved by the described method. At nominal frequency, the improvement achieved compared to the PLL-based method is minimal. The amplitude detection dynamic is similar but this last technic allows a better harmonic reduction when the amplitudes are very low (below 2V). This can also the noticed when the nonlinear load is disconnected. The controllers stop generating compensating harmonics very efficiently until the harmonics amplitudes decrease below 0.5V.

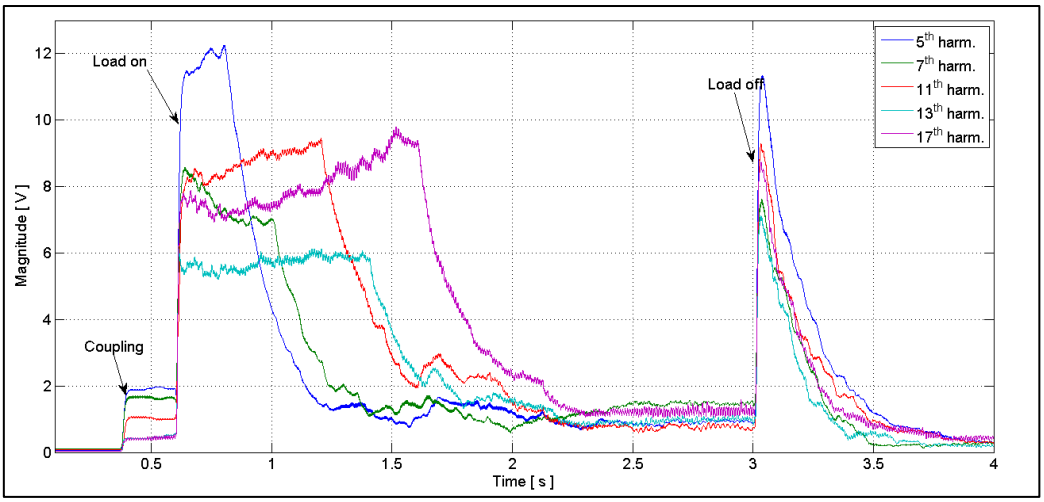


Figure 5-68: Inverter Frame-based Harmonics Magnitudes Control at Nominal Frequency

The major advantage appears when it comes to working at a frequency different from the nominal frequency. Similar to the PLL-based scenario, the grid frequency has been changed to its maximum value 50.5Hz. Depicted in Figure 5-69, the magnitude controls of the harmonics remain very stable also after the nonlinear load is disconnected. This is achieved without any controller coefficients optimization or the FIR filter phase-shifts correction. They are the same used in the magnitude regulation at nominal frequency. This reinforces the idea that the detection method is the major issue for the stability of harmonics compensation systems.

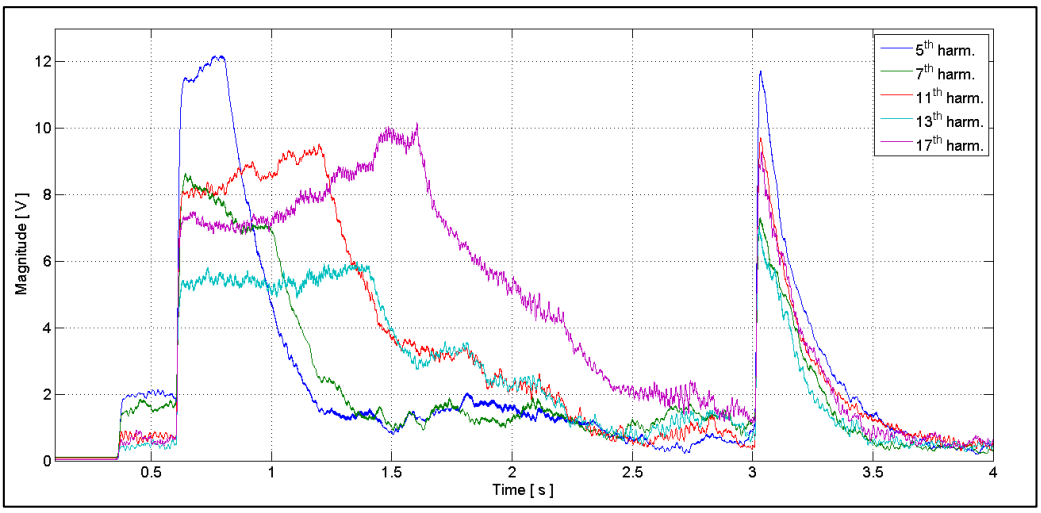


Figure 5-69: Inverter Frame-based Harmonics Magnitudes Control at Maximum Frequency

5.5.7 Power Inverter as power Grid Support and Harmonic Active Filter

In this part, the focus is no longer be set only on the harmonic content of the voltage but also on the power flow control between the inverter and the grid. This was intrinsically done during the harmonics compensation because the active and reactive powers were controlled to zero. Now in order to achieve a full grid support, the inverter power set points might differ from zero depending on the goal and the power control start automatically after coupling. The harmonics control method used here is the one based on the inverter reference frame for its stability and simplicity. The entire harmonics controller are simultaneous.

5.5.7.1 Inverter as Grid Support and Harmonics Filter by Pure Resistive Load

The non-linear resistive load is composed of a 5 kW resistor fed through a rectifier bridge. It is turned on after 0.8 sec and turned off at the time 2 sec. A second and third resistive load with a power of 1kW and 2kW respectively are connected in parallel at 1 sec and will be connected one after the other from time 1 to 3 sec and from 2 to 3 sec respectively. Figure 5-70 presents the relevant system information revealing the performance of the system. The inverter power control is stable and robust within the defined conditions. Within a half second the inverter reaches the desired power output even after a sudden system state change such as the load change at the times 1, 2 and 3 sec. The power delivered to the load is the sum of the inverter power and that of the grid. Keeping the inverter power output constant leads to a power feed into the grid when the load does not absorb all the power delivered by the inverter. As for the harmonics magnitude control, it successfully mitigates the harmonics not only when the nonlinear load is turned on but also after it is turned off. So it does not represent any instability factor for the system. Once the non-linear load is activated, it induces a reactive distortion power that decreases with the harmonics level.

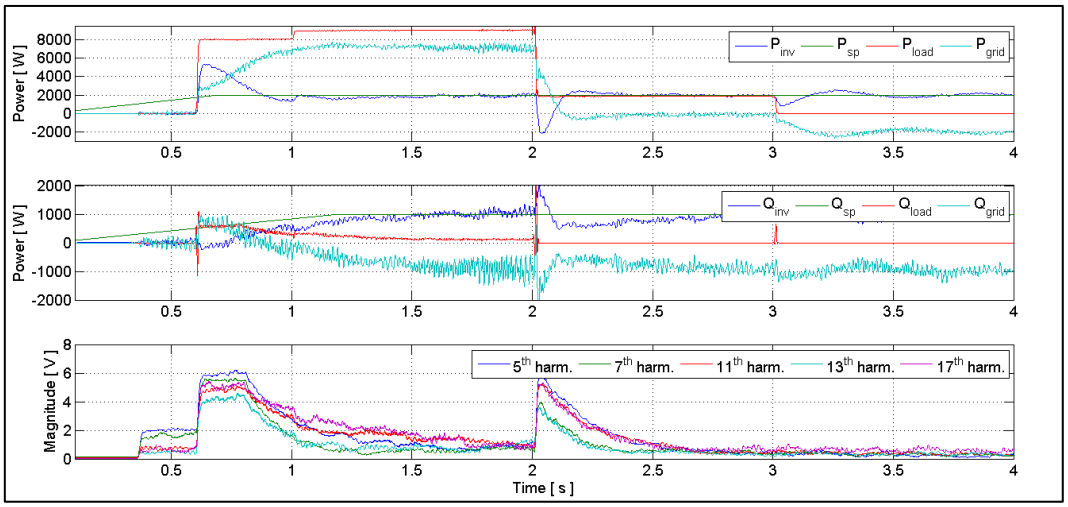


Figure 5-70: Inverter Power and Grid Harmonics Magnitude Control with Pure Nonlinear Resistive Load

5.5.7.2 Inverter as Power Factor Controller and Harmonics Compensator

In this scenario, the inverter is in charge of providing all the reactive power needed by the load. The load is composed of a pure nonlinear resistive 5kW load fed through a rectifier and turned on from time 0.8 to 2 sec. A second load but linear being resistive and inductive with 1kW and 2kVar as active and reactive power is connected from time 1 to 3 sec and last one, also a resistive and inductive load is switched on from time 1.5 to 3 sec with 1kW and 1kVar as active and reactive power respectively. Figure 5-71 depicts the control performance of the system. The harmonics magnitudes are successfully reduced to nearly 1V. As desired, the grid reactive power is kept to zero during the steady states. This means, all the required reactive power by the load is delivered by the inverter. Moreover, this concerns not only the distortion reactive power but also the inductive and capacitive reactive power. As the nonlinear load is disconnected, a disturbance is noticeable on the reactive power control but is rapidly corrected by the power control since the harmonics controllers are progressively reducing the level compensating harmonics they inject into the system.

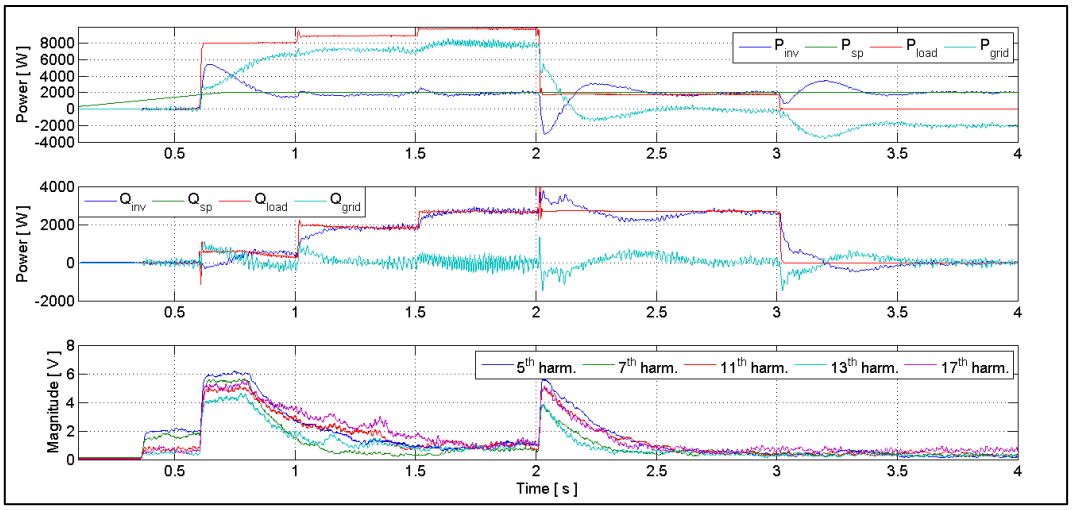


Figure 5-71: Inverter Power Control as Power Factor Corrector and Harmonics Compensator with Reactive Loads

5.5.8 Conclusion

Synchronizing two different power sources can be done using different methods. The standard methods based on PLLs works well but presents some weaknesses in terms of usefulness once the voltage sources are coupled. In order to control the power flow between the sources, an additional PLL (on the inverter input reference signal) is necessary. Furthermore, the PLL itself is an independent virtual frame whose internal controller has its own dynamic. So this might cause some delay, especially during transient phases. The synchronization based on the inverter frame presents more advantages compared to the PLL-based. The direct and quadrature components computed during the synchronisation step remain fully used during the power control. From these values, the phase shift between the inverter frame and that of the PCC is easily deduced. Furthermore, working with the inverter frame provides an important information for the harmonics compensation system that uses the inverter phase angle to deduce those of different harmonics voltages. It allows, for each harmonic, a reduction of the computation steps to determine their rotating frame (compared to the single harmonics PLLs).

The proposed impedance estimator has shown convincing results not in determining the right impedance of the load between the interconnected voltage sources but in finding the right impedance angle for decoupling the active and reactive power controls. Its output values would match with the real values if the input values (voltages magnitudes, phase-shift and exchanged active and reactive) were exactly known. Because it is almost impossible to extract the real voltages parameters once coupled, the estimator provides indeed inaccurate values but whose variations reflect only to a certain proportion, the power interaction between the grid and the inverter. The power control is therefore operated not in the real impedance frame but in a shifted one where the active and reactive power remain decoupled.

The simultaneous power control and harmonics compensation present finally no issue. The harmonics compensation eliminates the distortion reactive power, which affects the power control if the harmonics source changes. Nevertheless, the power controls remain stable and recover very well when it happens.

6 Experimental results on the test bench

In order to validate the developed APF on a real system, a complete test bench has been built up in the lab of the university. This chapter gives in details the characteristics of each element used in the lab, how they are connected together to simulate different scenarios and most importantly the achievements on the harmonics reduction and power control of the system.

6.1 Test-bench Setup

The test bench at the UL is made of multiple elements combining a synchronous machine generating the grid, a DC-fed power inverter, a full wave bridge rectifier and resistive loads. These elements are networked together in such a way that the loads can be fed either by the synchronous generator only or by the inverter only or also by both power sources when they operate together as grid-tied as depicted in Figure 6-1.

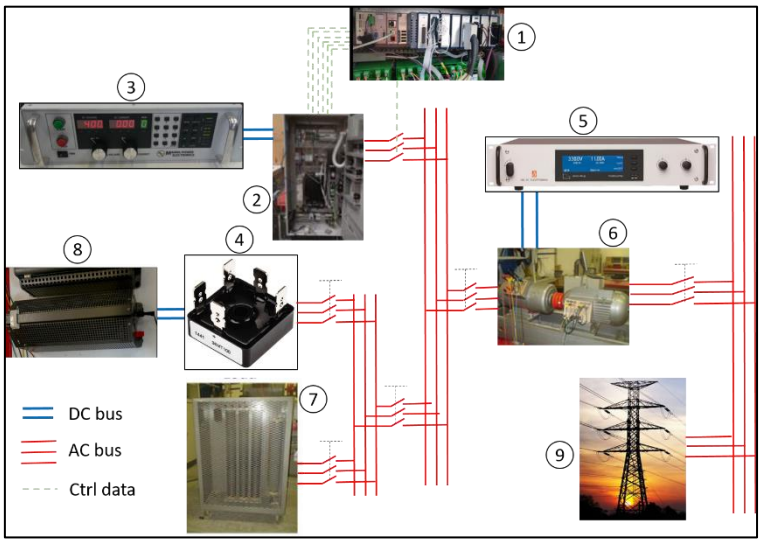


Figure 6-1: Micro Grid Test Bench Setup at the UL

The different components of the test bench are listed below:

1. Microcontroller
2. Power inverter
3. Controlled DC power source
4. Three phase bridge rectifier
5. Controlled DC power source
6. Synchronous generator
7. Three phase resistive load
8. DC resistive load
9. Main power grid

6.1.1 DC Voltage Source

Ideally, the foreseen DC power supply for the APF is batteries fed by for example a PV plant or wind turbine. This has been simplified to an electronic programmable DC power supply as shown in Figure 6-2. Constructed by Magna-power Electronics, it has a maximum power of 15kW with 1000V and 15A as maximum voltage and current. It requires a three-phase 380 Vrms input voltage and delivers the desired voltage with 88% efficiency with 350m Vrms ripple voltage [94].

Figure 6-2: DC Power Source TSD1000-15/380 from Magna-power Electronics

6.1.2 Microcontroller

The central piece of the whole system is a cRIO-9082 controller (CompactRIO) from National Instruments NI. It is a modular embedded controller featuring an FPGA of type Xilinx Spartan-6 LX150 and a real-time processor. The microprocessor is a 1.33 GHz dual-core processor with 2GB Ram and 32GB storage memory. Up to 8 different input/output modules, compatible with the chassis can be added. The microcontroller is programmable using LABVIEW [95]. The FPGA has a maximum clock frequency of 40 MHz.

Figure 6-3: NI cRio-9082 Controller

6.1.3 Passive Low-pass Filter

The inverter PWM output voltage is filtered through an LC passive filter from EPA (Figure 6-4). The capacitance triangle branch as depicted has been changed to the star connection in order to have a reference point especially when the inverter is to be synchronized to another voltage source.

Figure 6-4: SFAF2-400-40 Sinusoidal Filter of EPA

The filter has a nominal current of 40A with 400V nominal voltage. An inductance of 1.58mH and 7µF of capacitance. At nominal power, the voltage drop is about 5% while the power

losses are 168W. The fundamental frequency range goes up to 70Hz. The switching frequency ranges from 4 kHz to 16 kHz. The residual ripple voltage is approximatively 4 to 5% [96].

6.1.4 Bridge Rectifier

The rectifier used is a three-phase bridge rectifier from constructor VISHAY (Figure 6-5). The maximum output current is 35A with a 600V peak input voltage. The data sheet in [97] presents more details of the product.

Figure 6-5: Encapsulated Three-phase Full Wave Bridge Rectifier 36MT60 of VISHAY India

6.1.5 Synchronous Generator

In order to have no direct interaction with the main grid (in grid-tied operations), a synchronous generator is used to generate the primary voltages that are considered as a power grid. The generator, depicted in Figure 6-6 is has a maximum power output of 3 kVA with a nominal frequency of 50 Hz. It is externally excited in order to control the output voltage and this is done using a second electronic controlled DC source from DELTA ELEKTRONIKA (Figure 6-7). The DC power source can achieve up to 3.3kW power output with a voltage range from 0 to 330V and a current range from 0 to 11A. The efficiency at full load is 91% with a low level of ripple voltage of 10mV RMS [98].

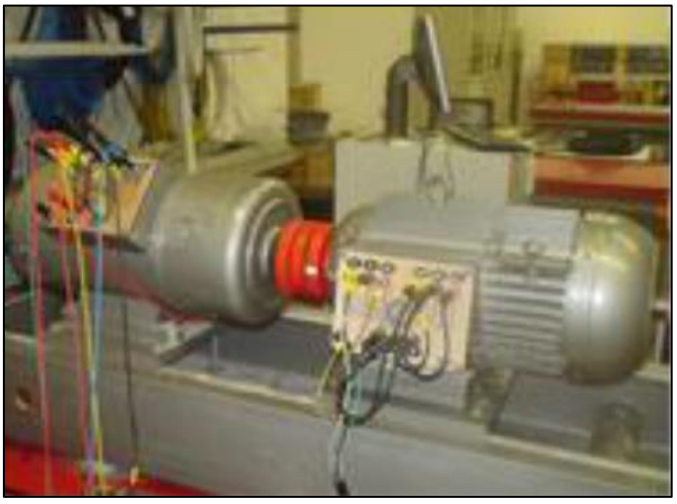


Figure 6-6: DC-exited Synchronous Generator

Figure 6-7: Controlled DC Voltage Source DELTA ELEKTRONIKA SM 330-AR-22

6.2 Implementation of the VSI Control in LabVIEW

As mentioned in paragraph 6.1.2, the microcontroller used to realize the theoretically developed APF is the cRIO-9082 from National Instruments NI. The controller program has been realized using LABVIEW 2014 SP1 (version 14.0.1f3) and is organized on the two executable layers, the real-time (RT) and the FPGA, of the microcontroller. The RT processor is mainly responsible for relative slow tasks such as the voltages magnitude control, the impedance estimator or the data logging of relevant system information. The FPGA is dedicated to fast tasks such as the voltages and currents measurements data acquisition and filtering, the PWM as well as the generation of the IGBT´s firing signal. A punctual program is run on the PC layer to generate the coefficients of the different filters as well as to find the attenuation factor at their rated frequencies. Only the generated filters parameters for the filter design are downloaded into the FPGA. The PC-program is not necessary for the system to run the APF. Paragraph 8.4 provides detailed explanations of some special code written or procedure taken, in order to get the whole system running. All the sub-programs not delivered within the standard LABVIEW library are explained and the different modules used with the microcontroller for the data acquisition and commands outputs are presented.

6.2.1 Program Structure

Figure 6-8 presents a full overview of the different tasks done by the RT and the FPGA including their frequency of execution. The closed loop control can be described in the following steps:

- **Measurements data acquisition:** at a rate of 20 kHz in the FPGA, the phase voltages and currents are measured.
- **Wave decomposition:** the measured voltage values are filtered by the fundamental (rated 50 Hz) FIR filter to extract only the fundamental components. At the same time, each harmonics FIR filter extracts its related harmonic wave from the voltage measurements.
- **Frame transformation:** after the filtering stage, the dq-decomposition (Clarke and Park transformation) occurs so that the direct and quadrature components of the fundamental voltage and the five first harmonics are calculated. The internal phase angle necessary for this transformation is provided by integrating, at the frequency 20 kHz, the actual angular velocity. The voltages and current dq-components are then available for the RT that processes them at a lower sampling frequency of 2 kHz for the fundamental voltage components control and 1 kHz for the harmonics voltages components controls. The difference of the control sampling frequencies reveals the control priorities set for the developed application. The most critical system state variable being the fundamental voltage is therefore monitored and controlled with a

higher precision compared to that of the harmonics magnitude control. The time constant of the PI controllers is determined by their proportional and integral coefficients.

- **System state control:** each harmonics component goes through its dedicated PI controller that computes its related compensating component value. For the fundamental voltage, different actions are taken if the system works grid-tied or off-grid. In the off-grid mode, the magnitude of generated voltage is controlled to 220V RMS through a PI controller that computes the magnitude of the reference fundamental signal. When the system is in grid-tied mode, not only the fundamental magnitude is regulated but also its frequency according to the power control scheme detailed in paragraph 5.5.5.2. The frequency PI controller generates actually a frequency variation value. All the controllers computed values are sent back to the FPGA.
- **Control signal construction:** the FPGA uses values (the harmonics compensating dq-components, the fundamental voltage magnitude and eventually the frequency variation) calculated by the RT to calculate the instantaneous value of each frequency. This is done by the inverse-Park and inverse Clark transformations and the internal phase angle. All the values are summed up together to determine the final instantaneous (three-phase values) control signal values.
- **PWM and firing signals:** a second loop in the FPGA is operating in parallel to generate the PWM firing signals using the intersection method. This runs at a frequency of 500 kHz in order to improve the calculation accuracy of the 15 kHz triangle carrier wave. The inverter firing signals are generated by comparing the controlled three-phase output voltage with the triangle voltage value.

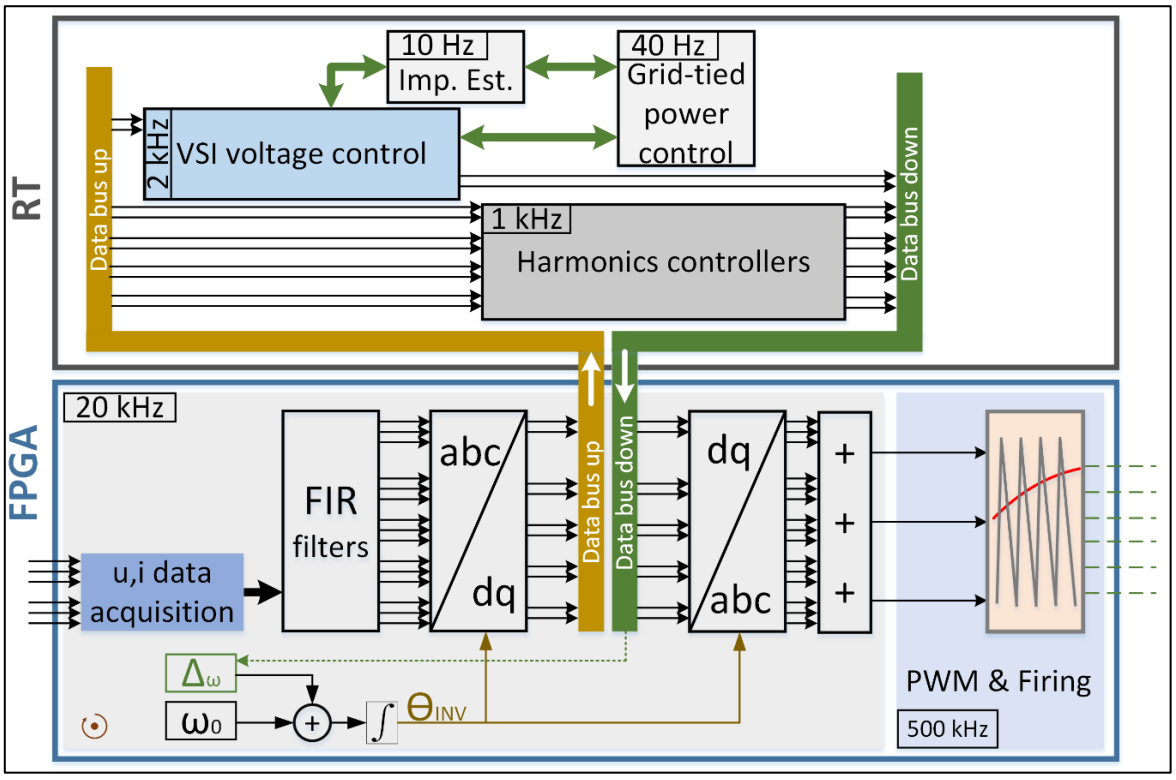


Figure 6-8: LABVIEW – Microcontroller Program Structure Organized between the Real-time and the FPGA

6.2.2 Different Program States

The inverter control has been programmed as a finite state machine as depicted in Figure 6-9.

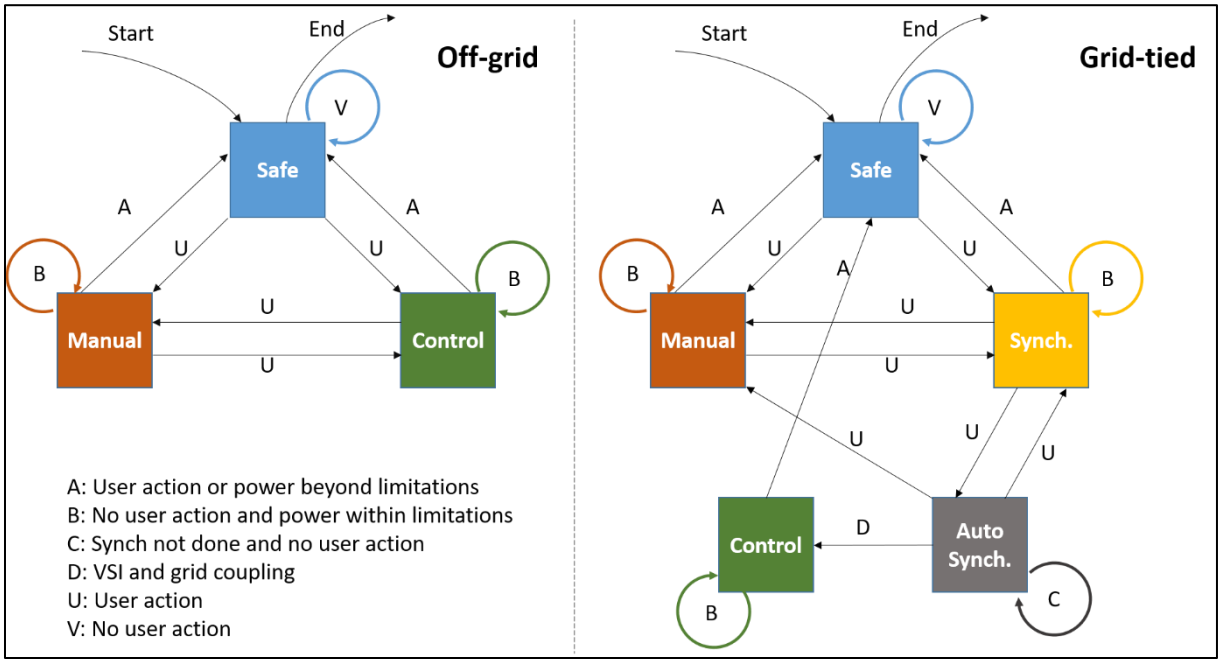


Figure 6-9: LABVIEW – Inverter State Diagram in Off-grid (left) and Grid-tied (right) Modes

In the stand-alone configuration, starting the program directly jumps into the safe state where the inverter generates no voltage and is disconnected from the grid. The user can for instance change to a manual run. In this state, the magnitude of the reference signal is manually set by the user. In the control mode, the magnitude of the inverter output voltage is controlled to 220V RMS. The user can change directly from one state to another. A power overshoot can bring the system back to the safe state. In the grid-tied mode, the safe and the manual states are similar to those in the stand-alone mode. For coupling the VSI to the grid, the program has to jump, either from the safe state or from the manual state, into the synchronisation state (user action). The synchronisation state allows the manual manipulation of the VSI output voltage using the graphic user interface (GUI). From this state, the user can choose as well the automatic synchronisation mode, where the system will automatically control the VSI output voltage to match that of the grid. Once synchronised, the two voltage sources are coupled by switching on the coupling relay on and the system jumps automatically into the control state. Unlike the control state in the off-grid mode where only the voltage magnitude is controlled, the grid-tied control state regulates the active and reactive power exchanged with the grid. The user or a power overflow can interrupt the process and make the system jumping back into the safe state. The final exit first causes the program jumping from any state into the safe state before stopping the program execution.

6.2.3 Real-time User Interface

A view of the RT GUI is described in Figure 6-10. Each highlighted section has a dedicated function but exchanges data with the other sections. The most important are the system configuration and the inverter voltage control. The harmonics control can be turned off without affecting the system basic functionality (only the harmonics compensation is switched off). The power control, as well as the control of the grid voltage magnitude, are only necessary for grid-tied operations.

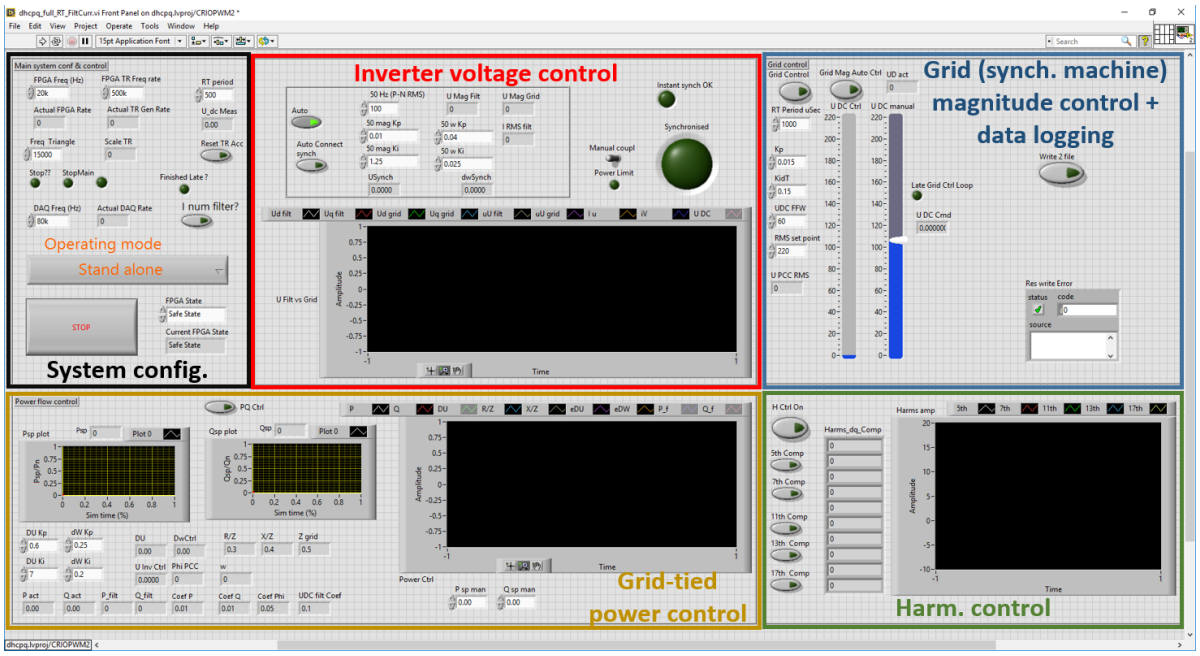


Figure 6-10: LABVIEW - Organization of the RT User Interface

6.2.3.1 System Configuration

This section allows the user to modify the basic configuration of the system such as the RT loop rate, the FPGA main and PWM loop rate, the frequency of the PWM triangle carrier signal and the most important, the working mode of the system that is either off-grid or grid-tied. The different states of the system, as well as the main stop button, are also included in this section.

6.2.3.2 Inverter Voltage Control

The final reference signal settings (magnitude and frequency) are indicated in this part. They are either manual inputs (in manual states) or automatically changed output values (in control modes). The grid voltage magnitude, the supplied current as well as the synchronization and coupling status are also shown there. The graph allows the visual monitoring and comparison of the inverter and grid voltages.

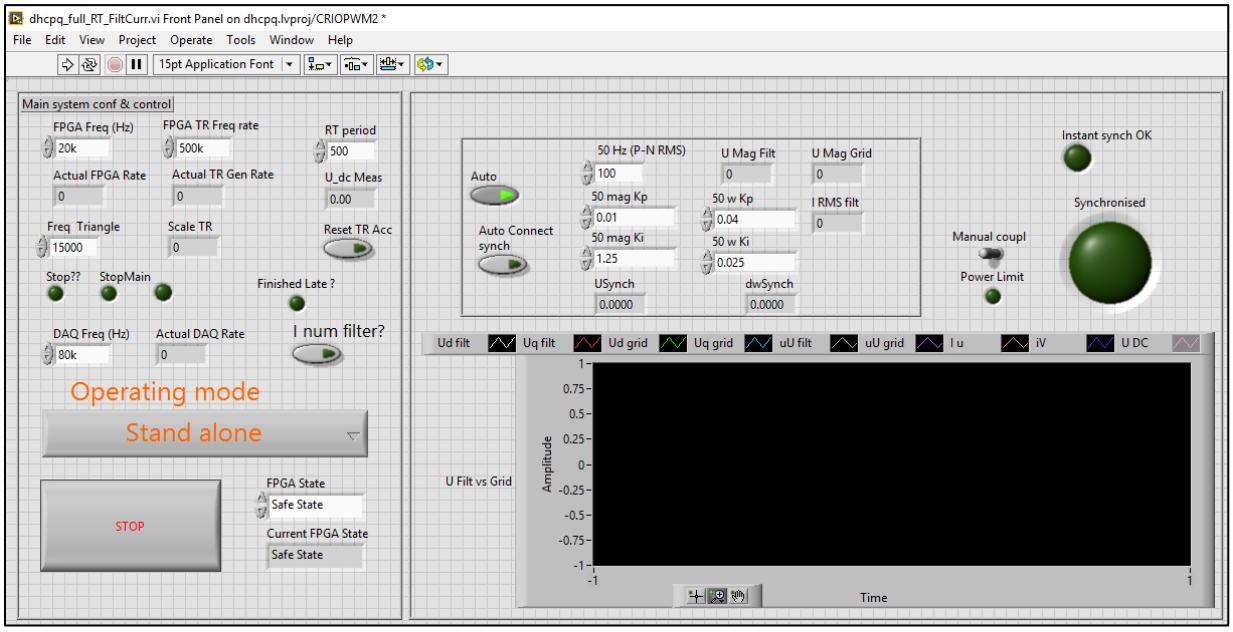


Figure 6-11: LABVIEW – View of the UI System Configuration and the Inverter Voltage Control Sections

6.2.3.3 Grid-tied Power Control

This section is mainly used when the inverter is connected to the grid as it includes the impedance estimator input and output values, the active and reactive power delivered by the inverter and their set-points. The section includes also the power PI controllers that modify the inverter voltage magnitude and phase as well as a graph to visualize mainly the powers exchanged between the inverter and the grid. In off-grid operations, only the plotted measured active and reactive powers exchanged with the last represent the most relevant information.

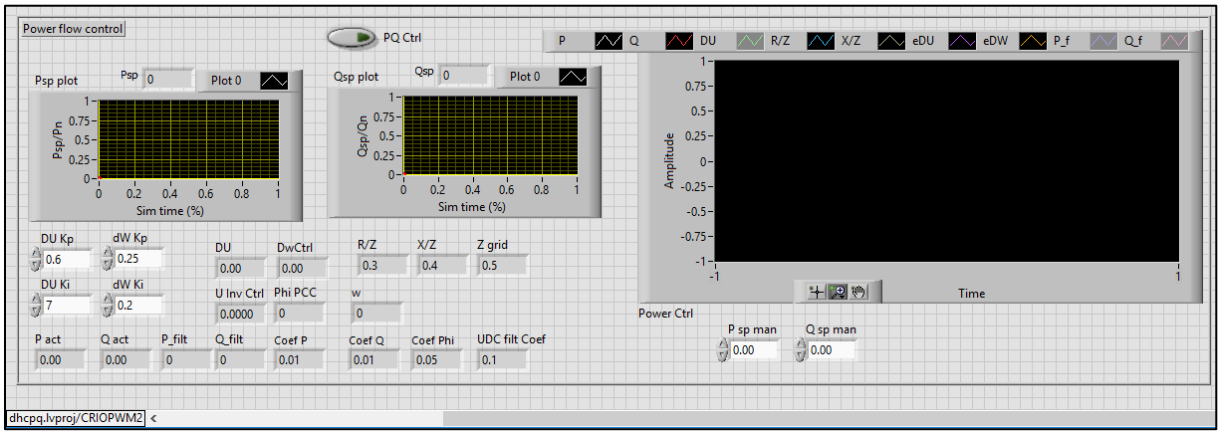


Figure 6-12: LABVIEW – View of the UI Grid-tied Power Control Section

6.2.3.4 Harmonics Control Section

The harmonics control section indicates which harmonics (among the 5th, 7th, 11th, 13th and 17th) are being compensated with a numerical array containing the compensating voltage dq-components for each harmonic. The graph beside displays the magnitude of the measured harmonic result of the compensation.

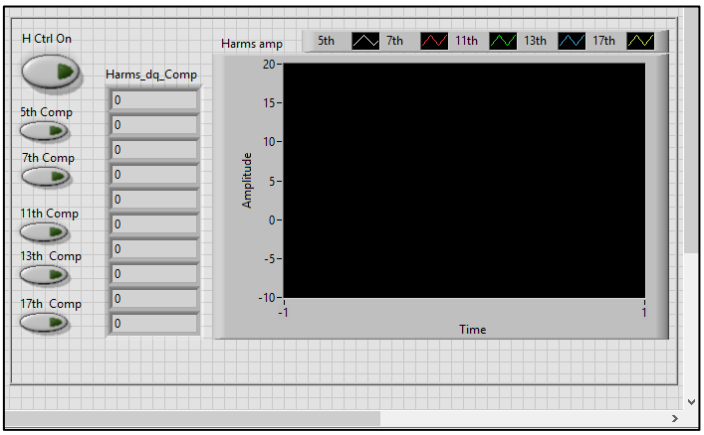


Figure 6-13: LABVIEW – View of the UI Harmonics Control Section

6.2.3.5 Grid Voltage Magnitude Control and Data Logging

In order to simulate a power grid in the lab, the test bench setup uses an induction machine as a motor supplied from the grid that is mechanically coupled to a DC-current excited synchronous generator (see paragraph 6.1.5). This section controls the magnitude of the generator terminal voltage by controlling the DC-current excitation. This can be done manually or automatically.

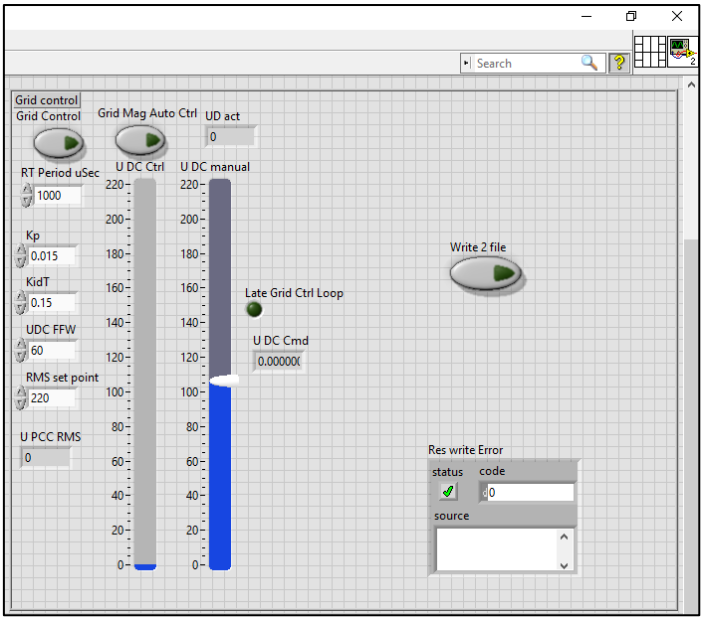


Figure 6-14: LABVIEW – View of the UI Grid Voltage Magnitude Control and Data Logging Section

An auxiliary button allows the user to record all 20 relevant information into a text file saved in the RT memory. The system records the values listed in Table 6-1 ten times per second.

Table 6-1: LABVIEW - List of Logged System Data

Variable	Unit	index	variable	Unit	index
Active power	W	1	VSI angular velocity	X π rad/s	11
Reactive power	VA	2	VSI actual voltage mag.	V	12
Filtered active power	W	3	Active power set point	W	13
Filtered reactive power	VA	4	Reactive power set point	VA	14
Grid impedance Z	Ω	5	Time (loop iterations)	X 1/10 s	15
Grid impedance ratio R/Z	-	6	5^{th} harmonic magnitude	V	16
Grid impedance ration X/Z	-	7	7^{th} harmonic magnitude	V	17
Phase diff. PCC vs VSI	rad	8	11^{th} harmonic magnitude	V	18
VSI Voltage mag. at coupling	V	9	13^{th} harmonic magnitude	V	19
Applied voltage mag. diff.	V	10	17^{th} harmonic magnitude	V	20

6.2.4 FPGA User Interface

Unlike the RT user interface, the FPGA interface (Figure 6-15) should not necessarily start along with the RT. The program is configured such a way that the FPGA runs in the background as the RT is started. Once the RT is stopped, so does the FPGA. That is the main reason why the FPGA interface plays a minor role and is developed mostly because of the visual programming language imposed by LABVIEW. Variables visible from the FPGA user interface are either written or simply read by the RT. For example, the state of the machine or some loop rates are written by the RT, while the voltages and currents measurements are acquired from the FPGA and read by the RT.

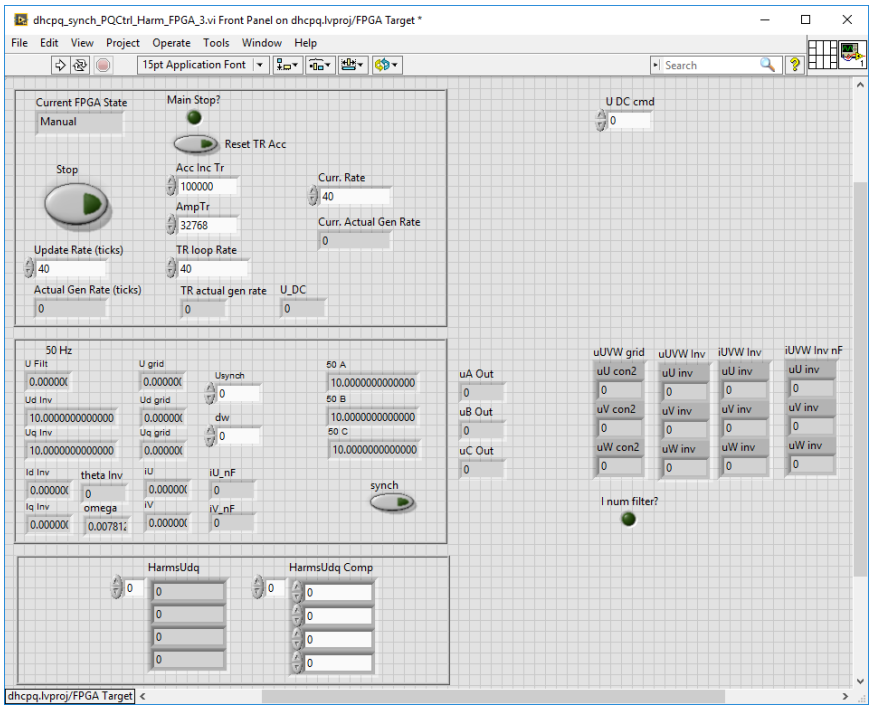


Figure 6-15: LABVIEW - FPGA User Interface

6.3 Test Bench Results

6.3.1 Power Inverter as Auto-compensated Voltage Source

In this experiment, the VSI feeds a resistive load through the rectifier as depicted in Figure 6-16. The total resistance of the load is 128 Ω and the maximum current is 5A. The output voltage is regulated to 220 V RMS.

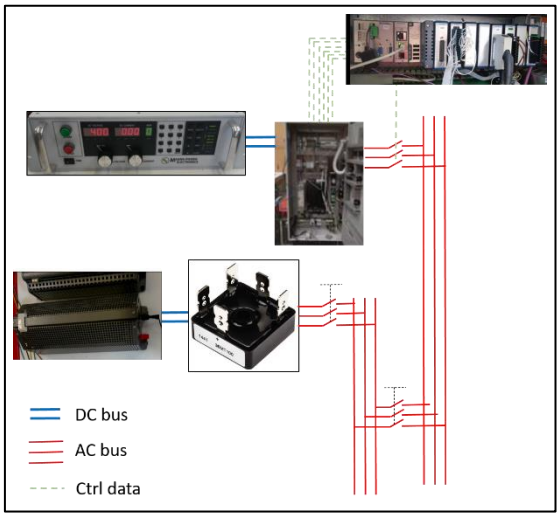


Figure 6-16: Test Bench Configuration – Power Inverter Feeding a Nonlinear Resistive Load

The experimental results of this setup are shown in Figure 6-17. The power flow clearly indicates when the load is turned on or off or if it is changed. Before the load is connected, the voltage is controlled to its nominal RMS value. Once the load is connected, the 7th harmonic voltage rises significantly compared to the others. It can be noticed that the harmonics mitigation works well as the harmonics magnitudes are progressively reduced to below 2V. The harmonic magnitude control reacts very well after the nonlinear load is disconnected and reconnected a short time later. Another checkpoint is the magnitude of the fundamental frequency. As the load changes, the RMS value of the voltage is impacted. It

decreases or increases as the load is turned on or off respectively. The magnitude control efficiently regulates within 4 seconds the voltage magnitude to its nominal frequency.

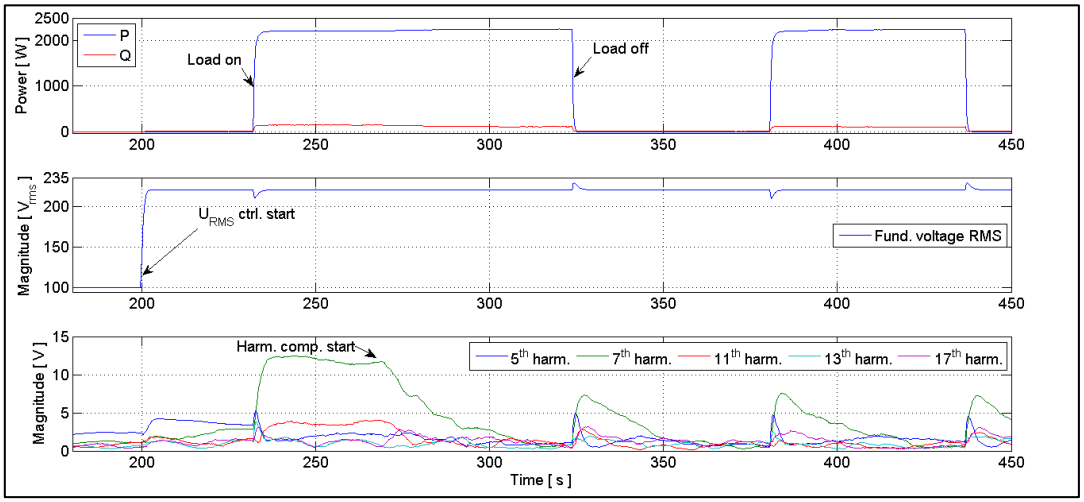
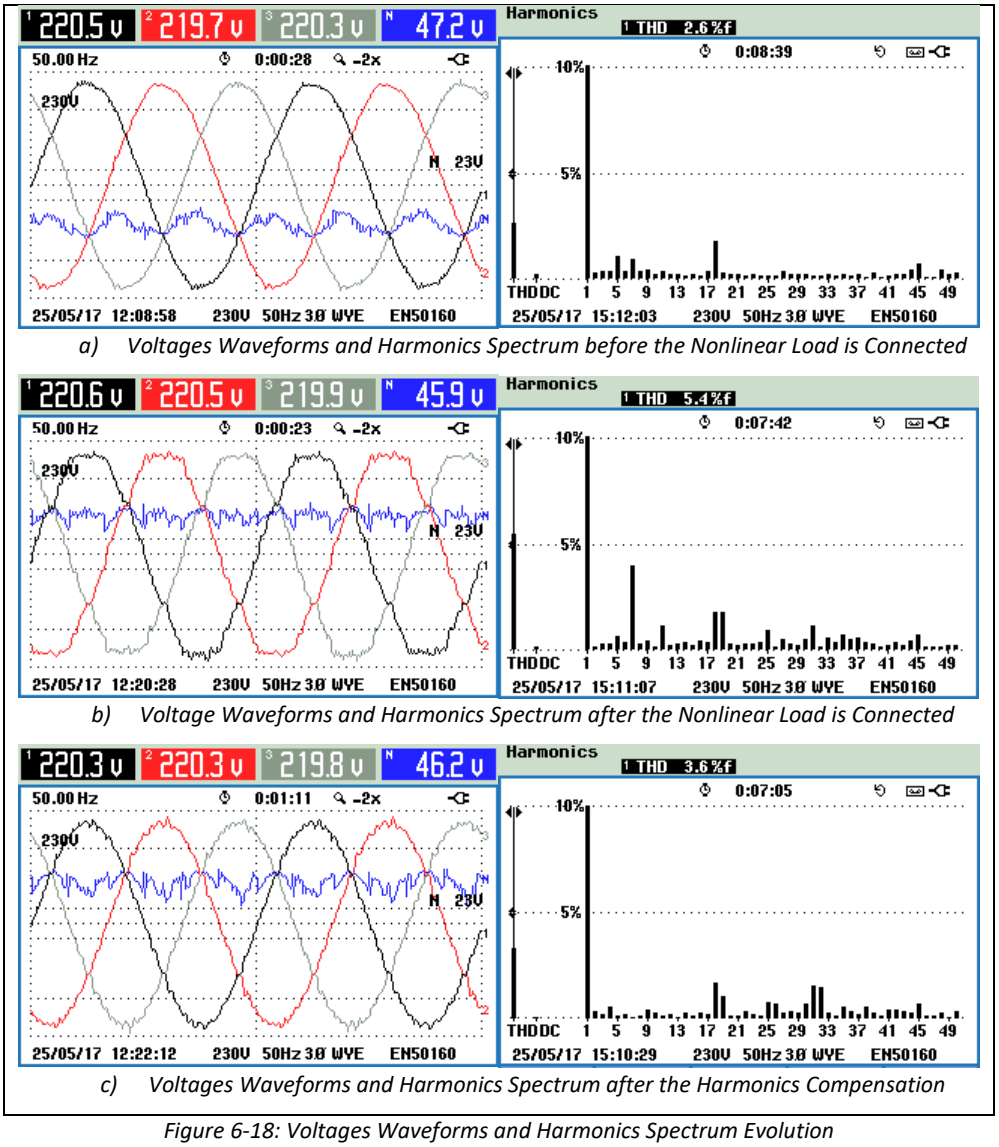


Figure 6-17: Experimental Results – VSI as Auto-compensated Voltage Source Feeding a Resistive Nonlinear Load



a) Voltages Waveforms and Harmonics Spectrum before the Nonlinear Load is Connected

b) Voltage Waveforms and Harmonics Spectrum after the Nonlinear Load is Connected

c) Voltages Waveforms and Harmonics Spectrum after the Harmonics Compensation

Figure 6-18: Voltages Waveforms and Harmonics Spectrum Evolution

Figure 6-18 illustrates the impact of the nonlinear load on the voltages waveforms. The measurement equipment used for these measures is the FLUKE 435 POWER QUALITY

ANALYZER. It corroborates with the previously described results. The unloaded (with no nonlinear load) and filtered output voltages of the inverter depict very good waveforms with a THD of 2.6%. Connecting the 2.2kW nonlinear load distorts the voltages and the THD nearly doubles its values to 5.3%. Also visible on the harmonic spectrum, the 7th harmonics has the highest magnitude. Once the 5th to the 17th harmonics magnitude control starts, it has successfully eliminated them and the waveform quality is improved by about 35%. The THD dropped from 5.3% to 3.3%. Despite the elimination of the 5th to 17th harmonic, the THD remains higher than the THD without nonlinear load. This is due to the fact that the distorted generated voltage that induces the elimination of the apparent harmonics influences the response of the nonlinear load with a direct impact on the magnitude of harmonics with higher frequencies that are not compensated.

A second experiment has been realized where the VSI feds not only the nonlinear resistive load but also a second linear resistive load as depicted in Figure 6-19. The nonlinear load is the same as in the previous case. The second load is an adjustable three-phase resistor with a power of up to 3kW.

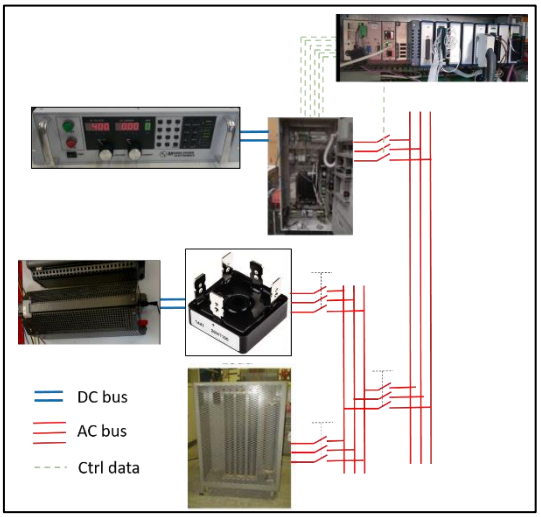


Figure 6-19: Test Bench Configuration – Power Inverter Feeding Multiple Nonlinear and Linear Resistive Loads

The results depicted in Figure 6-20 show how good the system responds to sudden load variations. Load 1 correspond to the rectifier fed resistance and load 2 to the three-phase adjustable resistor.

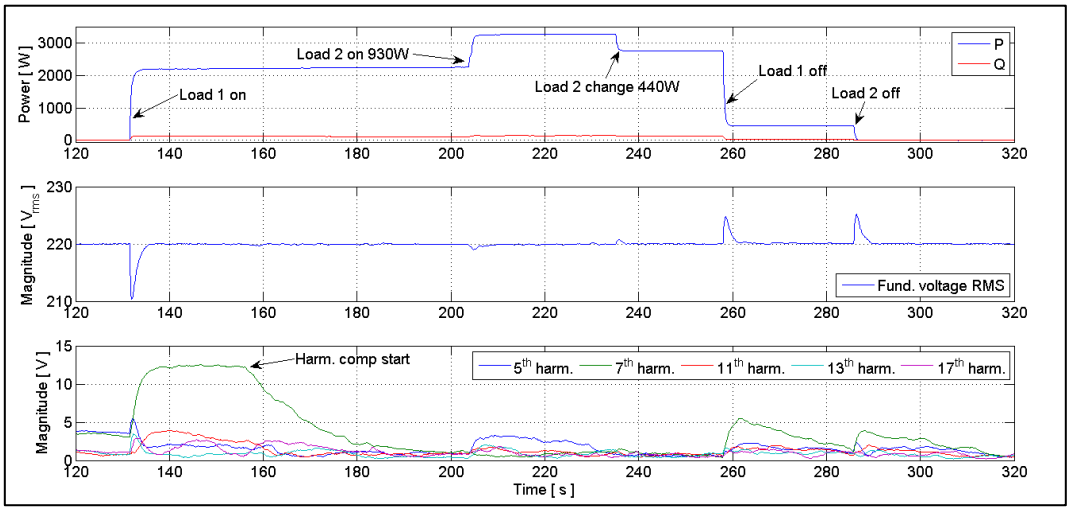


Figure 6-20: Experimental Results – VSI as Auto-compensated Voltage Source Feeding Multiple Loads

As before, the voltage RMS value is impacted since the 7^{th} and 11^{th} harmonics magnitude increase as the nonlinear load is switched on. The voltage control responds well to the disturbance. The harmonics level decreases as their magnitude control starts and remain active throughout the rest of the experiments. Switching the second load affects the harmonics as well as the fundamental voltage. The harmonics are successfully mitigated regardless the load variation and this also when there is absolutely no load.

6.3.2 Power Inverter as Grid Support and Harmonics Compensator

The electrical microsystem shown in Figure 6-1 depicts the complete configuration of the test bench used to demonstrate how the inverter can provide a considerable support to the main grid not only in participating in the total power feeding the load but also in improving (eliminating) the voltages harmonics appearing in the grid. The output voltage magnitude of the synchronous machine is controlled through the DC excitation voltage while the frequency depends on the asynchronous machine rotational speed. The power inverter is to be synchronised and coupled to the existing power system, must inject power into the system and also eliminate the voltage harmonics. The following lines present the results of different scenarios that have been tested.

6.3.2.1 Scenario 1: Inverter Coupled with an Undistorted Grid

The grid generated by the synchronous machine feeds a purely resistive load of 1.4kW. The inverter is coupled to the grid and its injected active power is gradually increased up to a maximum of 1.5kW. At this point, a 2.2kW non-linear and resistive load is switched on and the harmonics compensation starts few second later and remains active until the end of the experiment. After few dozen minutes, the nonlinear load is switched off. The inverter power gradually falls until zero. During this phase, the load drops a first time to 1kW and a second time to 0.5kW.

The very most important result is the decoupled control of the active and reactive power supplied by the VSI. This power control is based on the impedance estimator (detailed in 5.5.5.1) without which any controlled grid-tied operation would not be possible. Figure 6-21 depicts how well the virtual impedance estimator operates since the VSI active and reactive power have been perfectly controlled. The estimated cosine and sine of the impedance angle computed as R/Z and X/Z, are constantly readjusted as the load changes. The values do not always remain constant especially when the controlled power set points are both close to zero. A steady state of the estimator is reached once the active power is considerably higher than the active power that is controlled to zero. At this point, small variations of the generated active power have almost no impact on the estimate impedance angle. However, the power control remains stable despite the estimator oscillations. The impact of these oscillations is considerably mitigated by the voltage amplitude and frequency controllers. As expected, based on the calculations in 5.5.5, the estimated impedance angle does not reflect the real impedance since the estimated uses a wrong but reflective phase angle difference because the real phase shift between the VSI and the grid is unknown after both power sources are coupled. This can be observed on the plot after the load 2 (pure resistive but non-linear load) is switched on. The estimator depicts an increase of the inductance whereas the connected

load is essentially resistive. The same behaviour appears when the load 2 is turned off. The active and reactive power exchange between the VSI and the microgrid are independently controlled. Some interactions can be noticed during transient phases (variations of the load or the supplied power setpoint) but rapidly decay as the power controllers as well as the impedance estimator converge to their final values.

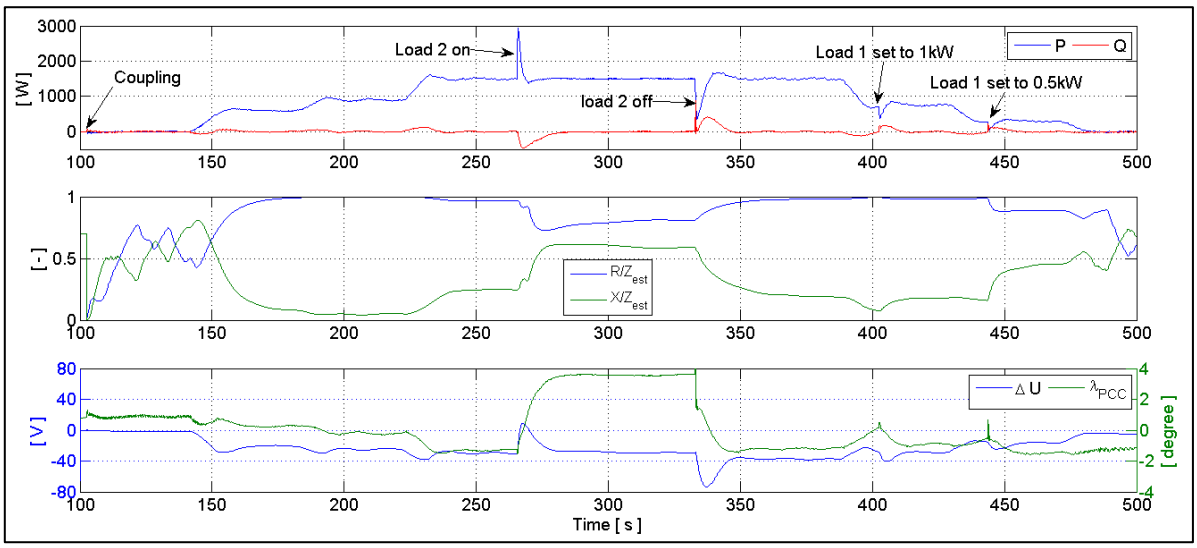


Figure 6-21: Experimental Results – Impedance Estimator Performance of the Grid-tied VSI

As mentioned before, the magnitude of the synchronous machine (generating the micro-grid power supply) is controlled. This means that the depicted power control parameters, which are the amplitude difference ΔU and the phase shift λ_{PCC}, are obtained from a tight interaction between the VSI controllers and that of the grid. Nevertheless, the power control remains robust and stable under the experimental conditions.

The second aspect to point out is the harmonics magnitude control depicted in Figure 6-22 where the voltage magnitudes of the 5th, 7th, 11th, 13th and 17th harmonics are controlled. Before coupling the inverter to the grid, a 1.4kW resistive and linear load is already supplied by the grid. Right after the coupling occurs and the power flow is controlled to zero, no measured harmonics remain very low. Once the VSI starts generating some power into the grid, the harmonics level especially the 7th and the 5th increase. This is caused by the generated PWM whose modulation index considerably increased (in relation with ΔU) until it reaches the overmodulation state. As the nonlinear load (load 2, at 2.2kW) is connected, it affects the harmonics in such a way that the 5th harmonic caused by the overmodulation is reduced while the 7th harmonics is increased along with the 11th harmonic. The activation of the harmonic magnitude control reacts as expected as it reduces the magnitude of the measured harmonics. Its major impact is visible on the 7th harmonic. However, the 5th and 11th harmonics magnitudes have also been reduced. Switching off the nonlinear load source of the harmonics causes some transient effects not only on the harmonics level but also on the power flow as well as the system voltage. The harmonics control successfully corrects itself so that there is no self-induced harmonic remaining in the system. It is also interesting to note that the harmonics compensation remains active after the nonlinear load is turned off and its effects are clearly visible when the harmonic levels are compared before (from time 230s to 260s) and after (from time 330 to 390s) the compensation at the same power level. The harmonics induced by the overmodulation are removed very well. The changes occurring later during the

experiment as well of the generated active power set point as of the grid load power also have an impact on the harmonics control since this last computation is based on the same reference frame as that of the fundamental frequency (used for the power control). As the fundamental frequency control (in this case only the power control) stabilizes, so do the harmonics compensations.

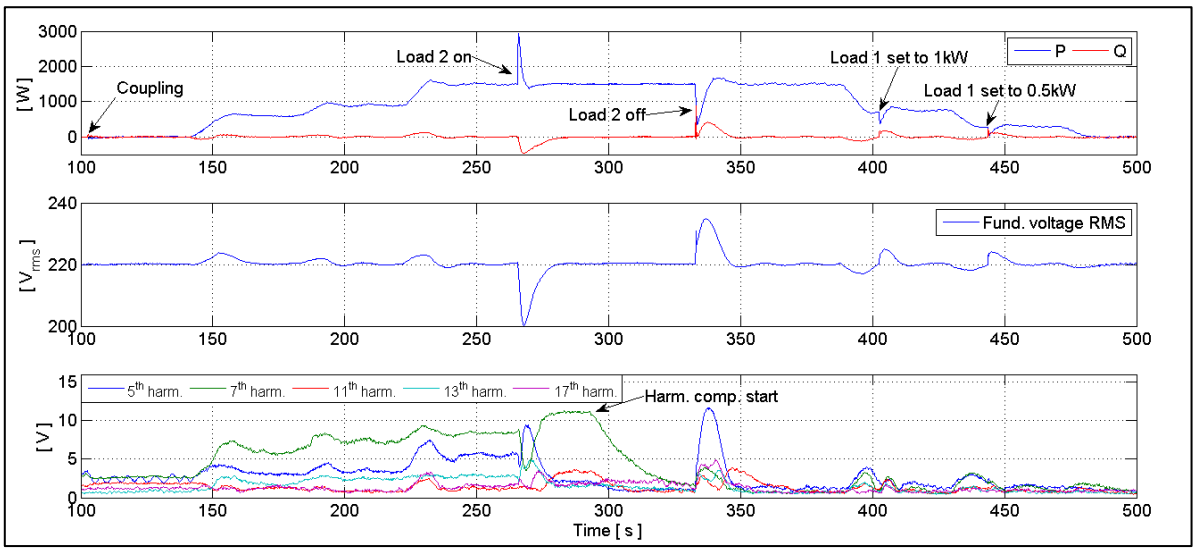


Figure 6-22: Experimental Results – Harmonics Magnitude and Power Output Control of the Grid-tied VSI

On the grid side, the magnitude control also performed well. The grid voltage magnitude remains in a constant range around the set 220 RMS value. It is impacted by the VSI power control dynamic as by the load variations.

A global view of the active power flow between the grid elements is depicted in Figure 6-23. These results are obtained from an external measurement equipment (FLUKE 435 Power Quality Analyzer). Once exported, they have been imported into MATLAB for further processing such as the Figure 6-23.

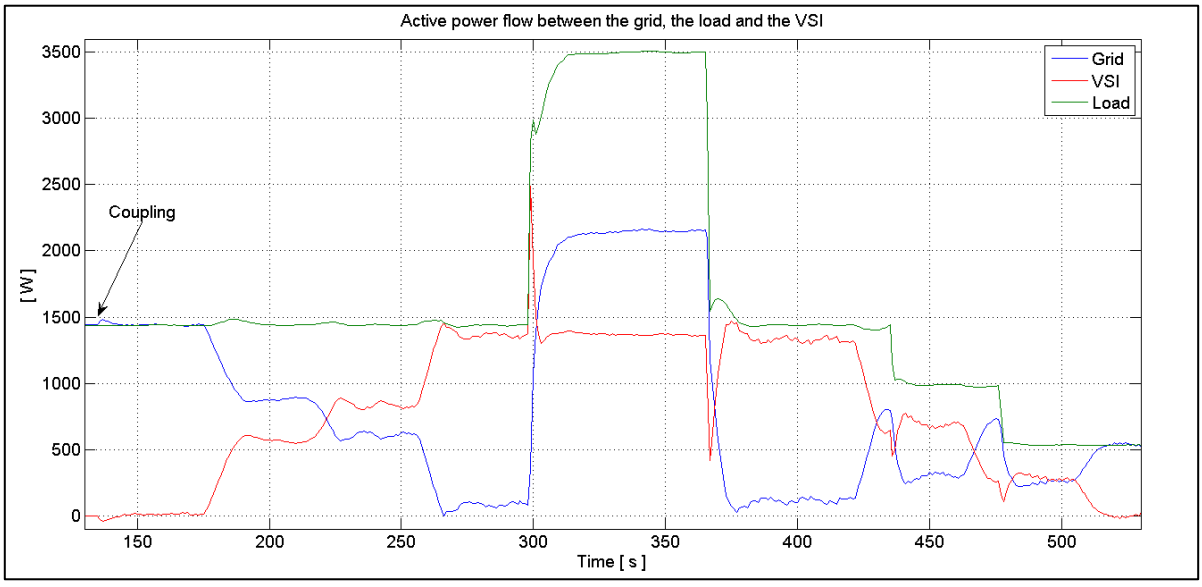


Figure 6-23: Experimental Results – Active Power Balance of the Grid-tied VSI

Once the VSI is coupled to the grid and its generated power regulated to zero, the grid supplies all the power drawn by the load. As the VSI increases its output power, that of the grid

automatically drops until nearing zero as the inverter supplies almost all the necessary load power. When the load is increased and the inverter power set to remain constant, the grid power jumps providing the missing power to meet the load requirement. Every time the inverter reduces its generated power, the grid instantaneously compensates until the power flow state where the inverter is totally passive i.e. generating no power, the grid is then fully supplying the load. Controlling the VSI until its passive state represents the most appropriate point to decouple the voltage sources if necessary.

6.3.2.2 Scenario 2: Inverter Feeding Active Power into the Grid

In this experiment, the capability of supplying some power to the grid is studied. The resistive linear load is held constant at 1kW. The VSI power control is set to supply more than the power consumed by the load for one period. Figure 6-24 is very similar to the results (Figure 6-22) in the previous scenario. It depicts the good harmonics control as well as the stable fundamental voltage magnitude of the system. Despite the self-induced harmonics due to the overmodulated fundament voltage, the system auto-corrected itself as the harmonic compensation started. The major noticeable point is depicted in Figure 6-25 where it can be observed how the grid responds to the power input of the VSI. When the load is fully fed by the grid (no power supplied by the VSI), the grid (synchronous generator) voltage frequency is as low as 49.2 Hz. As soon as the VSI starts supporting the grid by supply some power, the system frequency increases proportionally to the VSI input power. As the inverter-supplied power nears the load demand, the grid-supply power tends to zero and the frequency to 50 Hz. Beyond the load's need, the VSI power will inject power into the grid and the grid's frequency increases beyond 50Hz. During the experiment, with a constant load, the VSI has respectively supplied a maximum 1kW and 0.6kW to the load and the grid successfully. As the VSI power control progressively reduces the delivered power, the grid increasingly takes over the supply of the load while its frequency decreases.

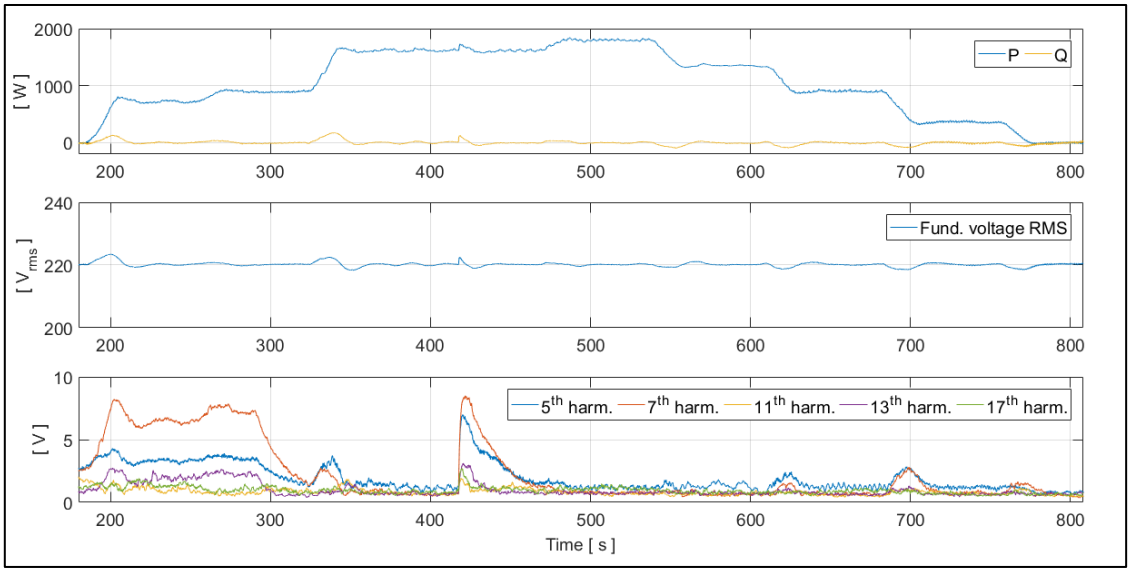


Figure 6-24: Experimental Results – Harmonics Magnitude and Power Output Control of the Grid-tied VSI Feeding the Grid

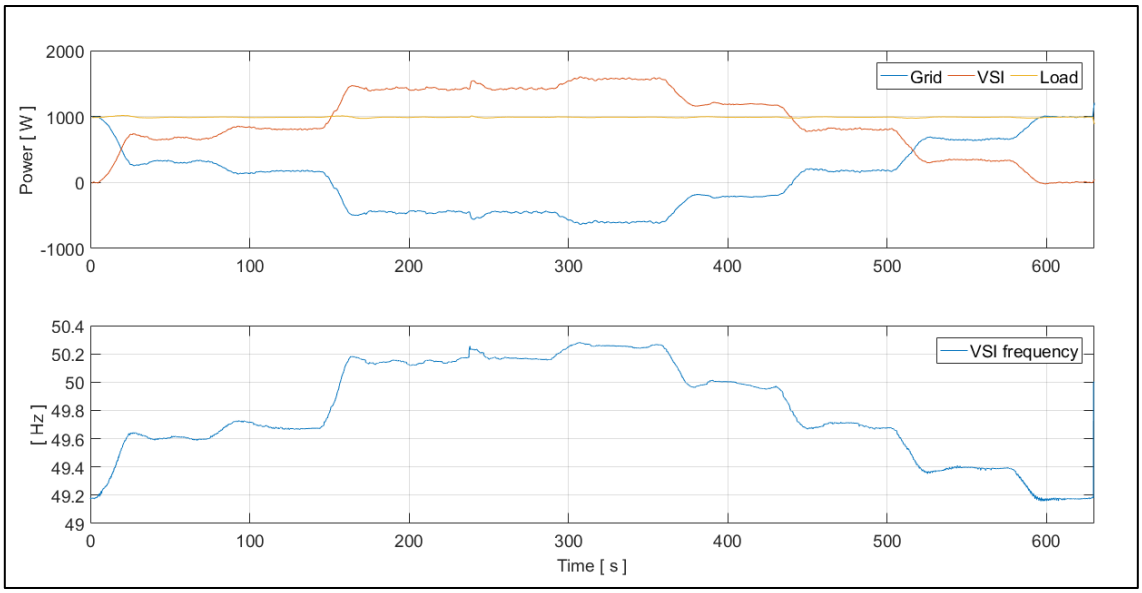


Figure 6-25: Experimental Results – Active Power Balance and Frequency of the grid-tied VSI Feeding the Grid

7 Conclusion and Perspectives

The electrical power quality is a multi-criteria definition of how well the electrical power supply is achieved. A continuous progress is happening in the field of manufacturing engineering for several types of equipment necessary to build up a power grid from the power production to the power distribution. This has allowed the reliability and availability aspect to represent a less and less critical point compared to the supply quality. Therefore almost all of the countries (certainly all developed countries), that have upgraded their power grid hardware are more concerned about the quality of the supplied voltage. In other places, still relying on aged equipment, the supply quality is far for being the main deciding criterion since the power supply is not yet reliable enough. Nevertheless, all countries are targeting an excellent power quality even if the sequence of actions to be taken one after the other may vary from place to place. However, natural disasters like earthquakes, hurricanes and lightings are uncontrollable negative factors of the power quality and represent the ultimate achievable minimum disturbance level.

Harmonics, among the different disturbances affecting the quality of the power supply, are the only power issue that is of increasing concern with the time (technologic progress). Boosted by the development and usage of more and more electronic devices especially by the final power consumers, the harmonics have become a critical voltage disturbance for low-voltage grids. Moreover, the spread of more and more decentralized power generation from renewable energy sources increases the potential impact of harmonics on other consumers since the filtering effect of the big and robust centralized grid is reduced. Electronic-based active power filtering is increasingly becoming the standard harmonic mitigation technic due to its flexibility concerning not only the range of harmonics frequency to mitigate but also the level of the load of the grid. Furthermore, active power filters are not as bulky as passive filters and can serve as more than simple reactive power compensators as they can also inject or consume active power into and from the grid.

The goal of this research project was to develop and implement on a real test rig a new selective harmonic compensation algorithm for active power filter. Furthermore, the system must be able to work as a stand-alone auto-compensated voltage supply or as a grid-tied power support and harmonics filter. The basic idea of the initial topology was the detection and compensation of the harmonic voltages direct and quadrature components in independent dedicated phase-locked loops frames. Theoretical results obtained from simulations have shown the stability problem of the system especially when the system frequency deviated from the rated frequency in the system elements such as FIR band-pass filters and the PLLs. It has been carried out that the PLLs light robustness was the cause inducing the overall system instability. That is the reason why a second algorithm has been proposed where the PLLs frames have been replaced by frames directly deduced from the intrinsic well-known frame of the inverter. This improved method offers convincing results in terms of stability at various system frequencies and load behaviours. In order to use the system as a full grid-tied power unit including the harmonic filtering feature, a new synchronization technic as well as a pseudo impedance estimator have been implemented. The synchronization method requires less computational resources as it relies also on the intrinsic frame of the inverter. The direct and quadrature components of the inverter output

voltage of the inverter and those of the grid voltage are calculated in the inverter frame, they are then compared and the inverter voltage is controlled so that they match. The pseudo impedance estimator is the deterministic computation of the grid and inverter's resistance and inductance from the measured active and reactive power, the measure voltage phase-shift between the inverter inner frame and the voltage at the point of common coupling and the applied inverter voltage. This has allowed an excellent power flow control between the inverter and the grid, while the harmonic compensation algorithm runs in parallel. The designed APF has been successfully implemented on the test rig using the LABVIEW-based microcontroller platform cRIO-9082. Experimental tests of the APF running as a stand-alone power supply or grid-tied power support have depicted very good results. In the off-grid mode, the inverter is able to ensure the supply of the fundamental 50Hz voltage and simultaneously mitigate the harmonics appearing in the system as soon as a non-linear load is connected. When the harmonics-generating load is disconnected, the inverter reacts properly as it rapidly reduces its compensation to zero. The same robust behaviour concerning the harmonics compensation has been observed, when the inverter is run as grid-tied power support. Moreover, in grid-tied operations, the developed system successfully achieved a decoupled control of the active and reactive power flow between the inverter and the grid. The experiments have shown that the inverter could not only completely replace the grid power supply to the load by generating near the load demand but also feed the grid by generating more than the load power requirement.

However, the developed system is designed as a pure symmetric system that is also symmetrically loaded. The grid-tied operations of the system assume a very stable grid that may not shut down in any case. That is the reasons why the proposed system needs the following further developments:

- **Unbalance running state**: the proposed topology makes it not perfectly convenient for unbalanced working conditions either off- or on-grid. The voltage unbalance issue mostly caused by an unequal loading of the supply voltage phases, induces a higher complexity concerning the harmonics. A common unbalance indicator not only for the fundamental 50 Hz voltage but also for the harmonics voltage is the unexpected appearance of the 3^{rd}, 9^{th}, 15^{th} harmonic in the three-phase voltage system. Some deep design reconfiguration is necessary in order to integrate this issue. The fundamental voltage control should be able to generate non-symmetric three-phase voltages. The harmonics detection method along with the magnitude control algorithm have a more complex task as it might be able to compensate differently (in magnitude and phase) depending on the system phase. This might considerably increase (nearly double) the computational load required compared to the currently developed system. A very complicated situation and unfortunately a common situation that needs to be resolved happens when, in a three-phase voltage system, a rectifier is connected on phase 1. The induced harmonics will appear on the two other phases and eventually the neutral line. The best and targeted harmonic compensation final state would be a zero harmonics compensation on phase 2 and 3 and a full compensation only on phase 1. This requires a very efficient system design and program implementation on the microcontroller.

- **Grid islanding**: a complete voltage drop of the grid, on which the inverter is coupled, will completely disrupt the running power control. If not properly detected and handled, especially in the case where the inverter was feeding power into the grid at the interruption time, the inverter will increase its voltage to the maximum. This can represent a real danger for any unaware individual or system operator. Depending on the usage, the inverter can be completely stopped for example if it is used as a grid power support unit or can serve as an uninterruptible power supply as it jumps from the grid-tied state to the voltage controlled off-grid power supply. The islanding detection sensitivity and the inverter states response time must be carefully investigated.
- **Voltage system flexibility**: the currently designed and implemented system is realized and applicable only for a three-phase voltage system. The system can easily be adapted for a single-phase voltage system as all the principles are similar except the voltage dq-transformation in the inverter frame needs to be adapted for a single-phase voltage. The orthogonal static voltage β-component can be computed using the different techniques used for single-phase phase-locked loops. The same technique can be used for the harmonics identification also. The single-phase design necessarily requires less computing resources as the number of FIR-filters is reduced and the PWM simplified.

Once these above-mentioned complementary points are properly integrated, the final upgrade would be the implementation of the proposed inverter on an industry scalable support. This can be an all-in-one motherboard controller dedicated to the inverter application. Only the cables of the DC voltage source and the grid voltages are connected as input and output is a single or three-phase voltage cable.

A further interesting investigation point is usability of the estimated pseudo grid impedance. In fact, in grid-tied operations of the VSI, the estimated grid impedance components, which are the resistance and the inductance, are used only for the decoupled power control. They do not correspond to the real grid's impedance because of the erroneous input values (voltage magnitude difference and phase-shift). These values along with the absolute impedance value could be considered as the grid's state seen from the coupled VSI. In a power grid with several distributed power source similar to the developed inverter, the different observed grid's states, if shared, can serve as a control parameter where the reaction time, as well as the power generation share, could be in function of the observed grid state. For example, a VSI observing a very low grid's impedance value might be set to react slower compared to a second VSI measuring a higher impedance in order to preserve a good stability.

8 Appendices

8.1 Passive Power Filters Constructors on the Market

Table 8-1: Non-exhaustive List of Passive Harmonic Filter Constructors

Constructor	Rated Voltage [V]	Power [kW]	Efficiency [%]	Min. Target	Input Voltage Quality
ABB	LV-HV	>3 Mvar			
	http://new.abb.com/high-voltage/capacitors/hv/harmonic-filters				
AFP TRANSFORMERS	600-35000				
	http://www.afp-transformers.com/harmonic-mitigation-solutions.html				
APQ	240-690			THDi< 5%	
	http://apqpower.com/products/low-voltage/harmonics/low-pass-harmonic-filters				
ARTECHE	https://www.arteche.com/en/products/harmonic-filters-low-voltage				
Circutor	400 -480	2-120			
	http://circutor.com/en/products/power-factor-correction-and-harmonic-filtering/harmonic-and-emi-filters/lcl-series-detail#documentation				
Enerdoor	230-600	400			
	https://www.enerdoor.com/category/view/passive-harmonic-filter				
Epa	380-690	4-440		THDi<5% with THDu<2%	THDu<5%, Unbalance <3%, Δf<2 Hz
	https://epa.de/filter/de/produkte/harmonic-filter-oberschwingungsfilter/				
General Electric - Grid Solutions	MV-HV				
	http://www.gegridsolutions.com/AlstomEnergy/grid/products-services/product-catalogue/electrical-grid-new/electrical-substation-ais/power-compensation/harmonic-filter-reactor/				
Harmonics Limited	208-600	200-2500			
	http://www.harmonicslimited.com/products/genmax/				
LARSEN & TOUBRO LIMITED					
	http://www.larsentoubro.com/electrical-automation/products-services/products/low-voltage-products/power-quality-solutions/harmonic-filtering-solutions/				
Maschinenfabrik Reinhausen	http://www.reinhausen.com/desktopdefault.aspx/tabid-399/297_read-5004/				
Microelettrica Scientifica	http://www.microelettrica.com/en/products/resistors/filter/filter_5.jsp				
MIRUS inernational	up to 690	4-2600	99	THDi<8%	
	http://www.mirusinternational.com/lineator.php				
MTE Corporation	400 - 690	600-1350	97	THDi < 8% at 30% load; < 5% at full load	unbalance <1%
	https://www.mtecorp.com/products/harmonic-filters/matrix-ap/				
Power Quality International	240-600			THDu< 5%	
	http://www.powerqualityinternational.com/products/harmonic-mitigating-transformer-low-voltage				

REO	400-480	6-1200			
	http://www.reo.de/en/products/chokes/oberwellenfilter.html				
Schaffner	380 - 690 +- 10%	1.1-380	98	THDi< 5-10%	THDu<2%, unbalance <1%
	https://www.schaffner.com/products/power-quality/ecosine-passive-harmonic-filter/all-products/				
SDC Industries	400-660	50-300			
	http://www.sdcindustries.com/pages/hf_passive.php				
Siemens AG	380-690	200-500			
	https://mall.industry.siemens.com/mall/en/WW/Catalog/Products/10045377				
Transcoil					THDu<0.5%, unbalance <0.5%
	http://www.transcoil.com/Products/HGP-Passive-Harmonic-Filter.htm				

8.2 Active Power Filters Constructors on the Market

Table 8-2: Non-exhaustive List of Active Power Filter Constructors

Constructor	Rated freq. [Hz]	Rated Voltage [V]	Current Range [A]	Load balancing	PF Comp.
ABB		200-690	30-320	Yes	yes
	Selective Comp until 50th harmonic. Harmonic attenuation factor <97%				
	http://new.abb.com/high-voltage/capacitors/lv/power-quality-filters				
Amtech	50 +/-5%	415-600 +10%, -15%	30-220	Yes	Yes
	Selective compensation until 51st harmonic. Attenuation factor > 97% at rated current. Auto restart mode				
	http://www.amtechelectronics.com/product.aspx?psid=12				
APQ	60Hz or 50, ± 3	208 – 480 V	25-200		
	Target THDi<=5%				
	http://apqpower.com/products/low-voltage/harmonics/active-harmonic-filters				
ARTECHE					
	https://www.arteche.com/en/products/harmonic-filters-low-voltage				
Circutor	50 Hz / 60 (± 4)		25-200	Yes	Yes
	Selective Comp until 50th harmonic.				
	http://circutor.com/en/products/power-factor-correction-and-harmonic-filtering/harmonic-and-emi-filters/afq-series-detail#documentation				
Comsys AB	50 / 60 +-2%	208-480, 480-690	70-300	Yes	Yes
	Selective Comp until 49th harmonic. Harmonic reduction rate up to 98%. Flicker compensation, WUI (Web User Interface)				
	https://adfpowertuning.com/technology/power-quality.html				
Consul Neowatt	50 / 60 +-5%	400 -600 +10%, -15%	25-600	Yes	Yes
	Selective Comp until 50th harmonic. Harmonic attenuation ratio up to 96%. Losses 3% of rating power				
	http://www.consulneowatt.com/products/iora-3000/44/				
Danfoss	50/60	380-415 /440-480	190-400	Yes	Yes
	Target THDi<=5%, Works without LCL filter				
	http://drives.danfoss.com/products/vlt/low-voltage-drives/vlt-advanced-active-filter-aaf-006/#/				
Delta	50 / 60 +/- 10%	400-690	50-525	Yes	Yes
	Selective Comp. Until 31st at 690 V and 50th at 400 V. Filter up to 98% harmonics at rated load, THDu<3%, THDi<5% after filtering. Low thermal loss (≤3% of rated APF kVA), efficiency ≥ 97%. AC 400V: Mitigate negative and zero sequence, CC 690V: Up to 10 Racks(5 modules per cabinet)				
	http://www.deltapowersolutions.com/en/mcis/pqc-active-power-filter.php				
EATON	50 / 60 +- 3	380-480 +-10%	60-200		Yes
	Selective compensation until 51st harmonic. Configurable target THDi/THDu. Power losses: To 480 Vac <3%; to 690 VCA <5%				
	http://www.eaton.com/Eaton/ProductsServices/Electrical/ProductsandServices/PowerQualityandMonitoring/PowerConditioning/HarmonicCorrectionUnit/index.htm				

Enerdoor	50 - 60 +3%, -5%	400 - 690	25-150		Yes
	Reduces THD to 5%. Compensate up to the 50th harmonic. Overall efficiency > 97%				
	https://www.enerdoor.com/products/view/finhrma				
Enertec Power Solutions	50/60Hz ± 3		30-240	Yes	Yes
	Compensate up to the 51st harmonic				
	http://www.enertec.co.nz/active-harmonic-filter				
General Electric - Grid Solutions		400V + 15%, -20%			
	Max compensated harmonic: 50th				
	http://www.gegridsolutions.com/AlstomEnergy/grid/products-services/product-catalogue/electrical-grid-new/electrical-substation-ais/power-compensation/harmonic-filter-reactor/				
ICAR	50/60 +-3	200 -480 +-10%	60-300	Yes	Yes
	Selective compensation up to the 50th harmonic. Flicker compensation				
	http://www.icar.com/en/product/active-filters/				
LARSEN & TOUBRO LIMITED			30-600	Yes	Yes
	http://www.larsentoubro.com/electrical-automation/products-services/products/low-voltage-products/power-quality-solutions/harmonic-filtering-solutions/				
Maschinenfabrik Reinhausen	50 / 60	400-800	125-500	Yes	yes
	Selective harmonic compensation up to the 51st harmonic and above. Voltage stabilization via Q(U)-control, Flicker compensation				
	http://www.reinhausen.com/desktopdefault.aspx/tabid-1789/2508_read-7278/				
Merus power	50/60	200-480	50-200	Yes	
	Selective compensation up to the 50th harmonic. Losses <2.3%				
	http://www.meruspower.fi/products/active-harmonic-filters/				
Mesta Electronics	50/60 +/- 5%	208-600	50-300	Yes	Yes
	Target: TDD<5%				
	http://www.mesta.com/Active-Harmonic-Filters.html				
NZIND				Yes	Yes
	Selective compensation up to the 50th harmonic. Target THDu<3%, THDi<5%				
	http://nzind.co.nz/post/nzind-now-offer-a-full-range-of-power-quality-products				
Power Survey		480-690	100-300	no	no
	https://www.powersurvey.com/products/active-harmonic-filters/				
Rockwell Automation	50/60	400-690	170-265		yes
	http://ab.rockwellautomation.com/Drives/PowerFlex-755TL				
Schaefer			60-300	Yes	Yes
	Selective harmonic compensation up to the 49th harmonic. Flicker compensation				
	http://schaeferpower.com/content/portfolio/active-harmonic-filters/				
Schaffner	47 - 63	200-480	30 -300	yes	yes
	Selective harmonic compensation up to the 50th harmonic. Target THDi<=5%				

	https://www.schaffner.com/products/power-quality/ecosine-active-harmonic-filter/all-products/				
Schneider Electric	50/60, ±3	208-690 +/- 10%	47-300	yes	yes
	Selective harmonic compensation up to the 51st harmonic. Configurable THDi set point				
	http://www.schneider-electric.com/en/product-range/63426-accusine-pcs%2B?parent-category-id=4300&parent-subcategory-id=4340				
Schneider Electric	50/60, +/- 4	400 +15%, -20%	20-120	no	Yes
	Selective harmonic compensation up to the 50th harmonic. Harmonic attenuation >10:1 if load THDi<40%. Power factor correction, cos ϕ to near unity, selectable set point. Overload: possibility of continuous operation with current limitation				
	http://www.schneider-electric.com/en/product-range-presentation/2186-accusine-swp?parent-category-id=4300&parent-subcategory-id=4340				
SDC Industries	50/60 +/- 5%	208-240, 380-415 +/- 10%	30-60	Yes	Yes
	Selective harmonic compensation up to the 50th harmonic. Attenuation factor > 97%				
	http://www.sdcindustries.com/pages/hf_eaf.php				
Siemens AG	50/60	380-480	100		Yes
	Compensation up to the 16th harmonic, target THDi<3%. Complete description of filter function with analogue, time-continuous models: no FFT, no FIR filters				
	https://www.siemens.be/in/documentation/upload/documents/AHF_in_SIVACON_S8_eng.pdf				
Sinexcel	50/60 (45−62)	380 -690	25-600	Yes	Yes
	Selective harmonic compensation up to the 50th harmonic. Target THDi<=5%				
	http://sinexcel.com/en/product-6.html?gclid=Cj0KCQjwgIPOBRDnARIsAHA1X3Qst465KkWDNLgXUsMc7uceiidX5gplh8-5pWYYoZQgMxR68QH5WlwaAiq5EALw_wcB				
Staco Energy Products Co.		208-480	25-300	no	Yes
	Global harmonic compensation up to the 51st order				
	http://www.stacoenergy.com/				
TDK - EPCOS AG	50/60 ±3	180-528	60-300	Yes	Yes
	Compensate up to the 50th harmonic. Harmonic reduction rate up to 98%. Flicker compensation				
	https://en.tdk.eu/pqsine_presentation				
Transcoil		up to 600	up to 500		Yes
	Target TDD<5%, compensation up to the 50th harmonic				
	http://www.transcoil.com/Products/HGA-Active-Harmonic-Filter.htm				

8.3 Impedance Estimator Flow Chart

The flowchart presented below (Figure 8-1) represents the different main states of the VSI system when it is used as a grid support unit. The first state, which is the loop 1, represents the safe state (decoupled and inactive mode) where the system waits for the command to start the synchronization with the grid. The loop 2 corresponds to the synchronization phase. The VSI voltage is controlled to match the grid's voltage magnitude, frequency and phase. Once synchronized, the system automatically coupled the two voltages sources and jumps into the third and final mode that is the power control mode. The delivered active and reactive power are controlled by modifying the voltage magnitude, phase angle and the estimated grid impedance. The estimation of the grid impedance is performed based on the previously delivered powers (active and reactive) and the related VSI voltage characteristics (magnitude and phase angle). The system remains in this state until it is changed by the user for instance.

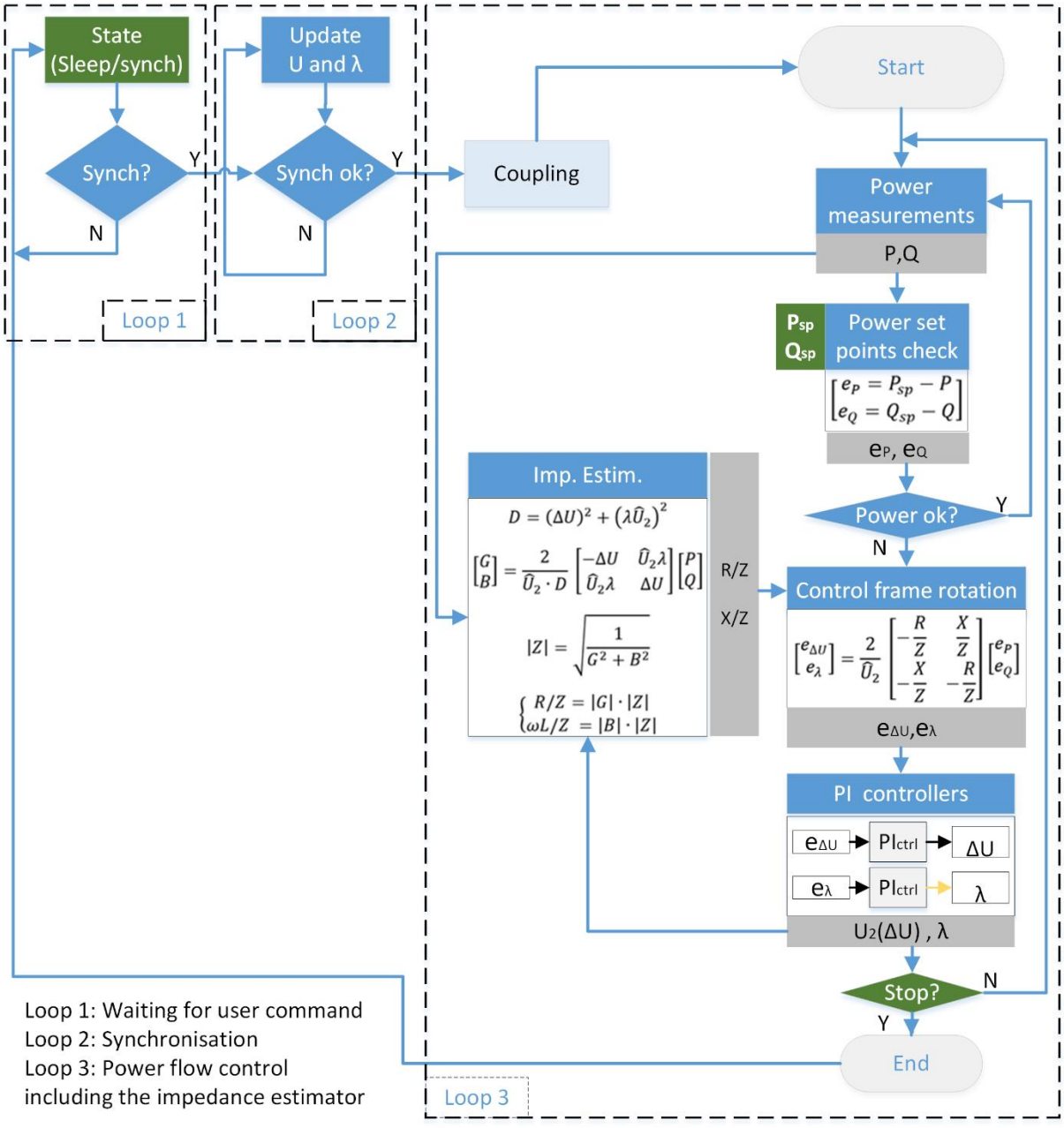


Figure 8-1: Power Control Flowchart Including the Impedance Estimator of the Grid-tied VSI

In real life conditions, the system should integrate various security check and safety procedures clearly defined. For example, the behaviour of the VSI if the grid experiences a voltage drop (below the standard limits) or even an interruption. Issues like anti-islanding should be taken into consideration and fixed properly.

8.4 LABVIEW Procedures and Codes Details

8.4.1 Create an FPGA FIR Filter in LABVIEW Using the IP Generator

Designing and using FIR filters in the RT is quite common and there are several tools available in the LABVIEW palette, the Digital Filter Design Toolkit. However, building an FIR filter that is functional in the FPGA is a bit more complex. The process can be described as follows:

- **Design and saving of a Fixed-point FIR Filter**: an FIR filter is designed on the PC using the Digital Filter Design Toolkit palette. The filter coefficients are then saved into a file.

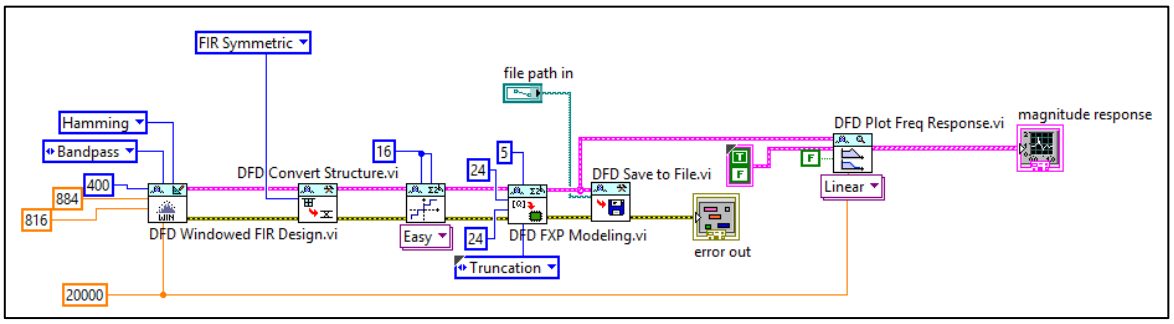


Figure 8-2: LABVIEW - Design and Saving to File of a Fixed-Point FIR Filter

The Figure 8-2 shows a possible process, how an FIR filter is designed and saved into a file. The designed filter is a 400-order band-pass filter with the bandwidth between 816 and 884 Hz (17^{th} harmonic frequency -850Hz $\pm$ 4%). The coefficients (to be generated) are 16 bits numbers with input as 24.5 fixed-point number and 24 bits output numbers. The filter runs at a frequency of 20 kHz. A further important information is the amplitude response (Figure 8-3) of the filter mainly near the rated frequency. The magnitude response coefficient is in this case 0.65245 at the rate 850 Hz.

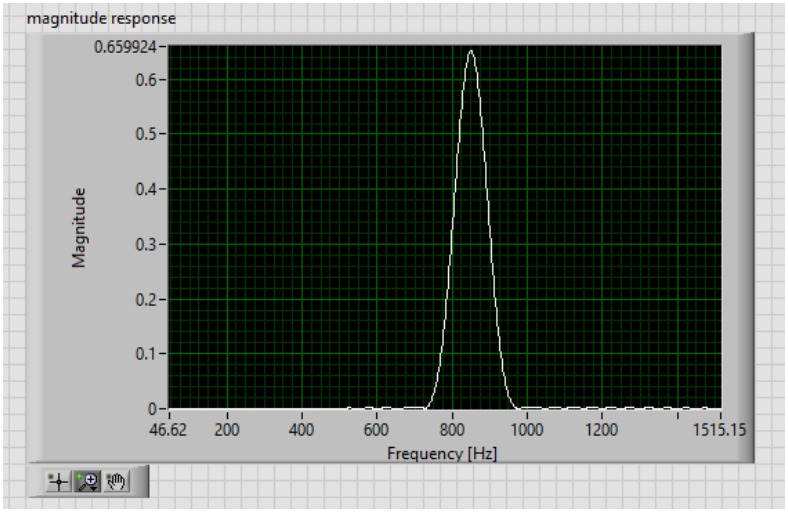


Figure 8-3: LABVIEW – Magnitude Response of the Designed FIR Band-pass Filter

- **Start the IP Generator:** The FPGA IP Generator tool can be opened through the contextual menu of the FPGA target embedded in the microcontroller. The Single-Rate Filter option has to be selected in the opened dialogue box.

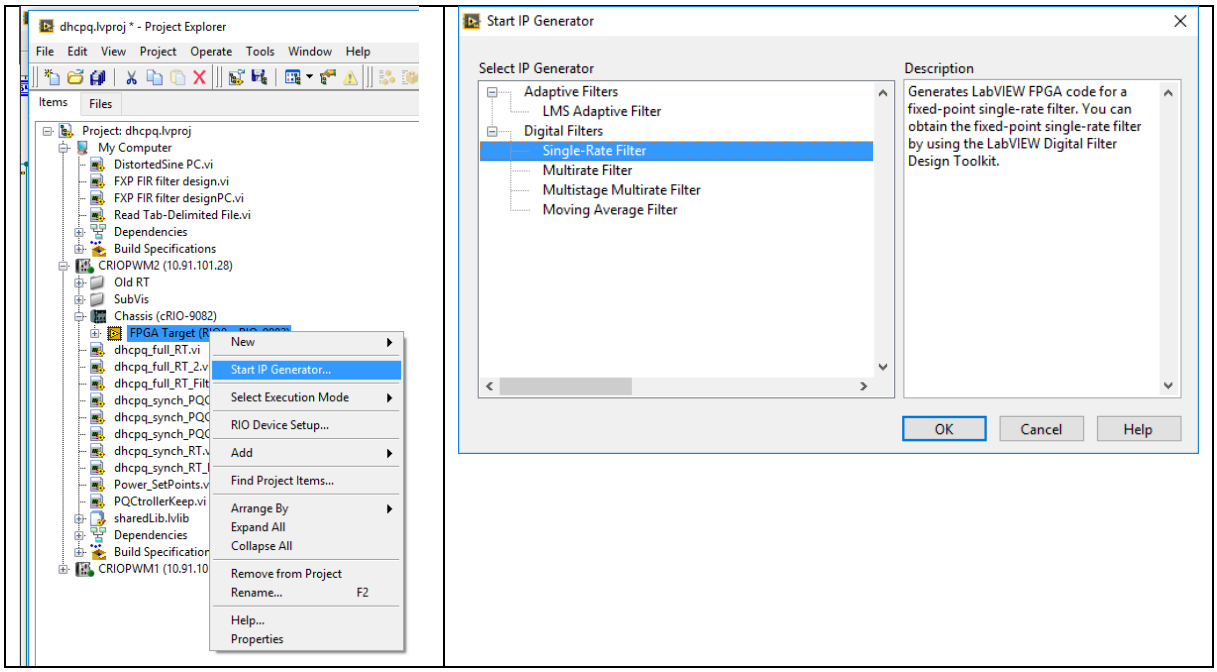


Figure 8-4: LABVIEW – IP Generator Starting Process

- **Filter configuration:** The configuration window of the IP Generator allows the user, as shown in Figure 8-5, to modify some characteristics such as the output data type, the rounding of the overflow mode. It is interesting to note that the input data type was automatically detected as defined during the generation of the filter file. Clicking on OK will start the final step, which is the build-up of the filter LABVIEW executable file (VI) with the indicated name in the configuration window.

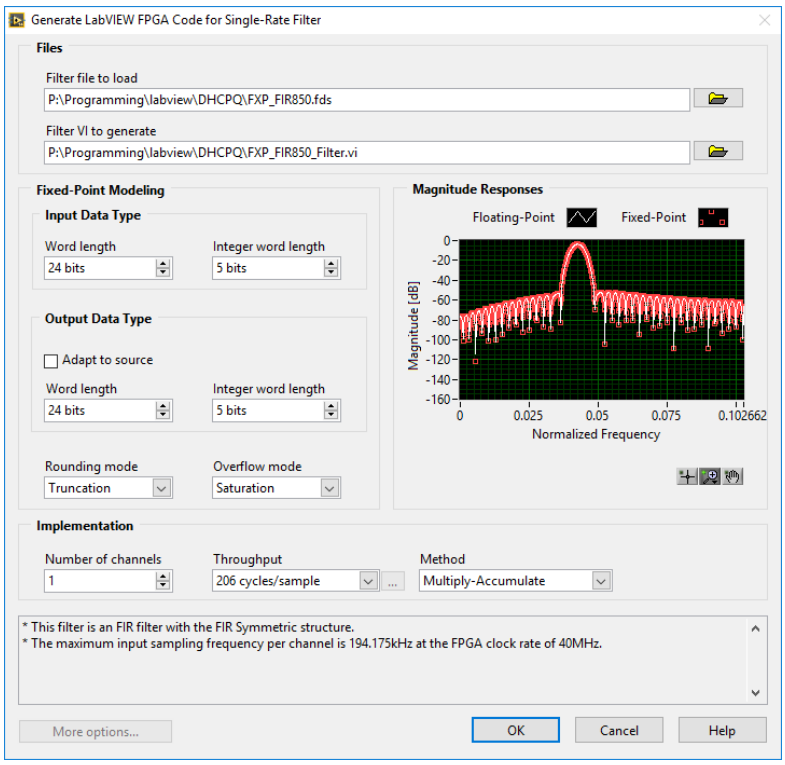


Figure 8-5: LABVIEW – Filter Configuration Windows of the IP Generator

- **Using the filter:** the generated filter VI front and back panel looks very simple as presented in Figure 8-6. However, in order to use the filter, the generated VI just

has to be inserted in the desired LABVIEW main VI. This is depicted in Figure 8-7 where two IP generated FIR filters are used.

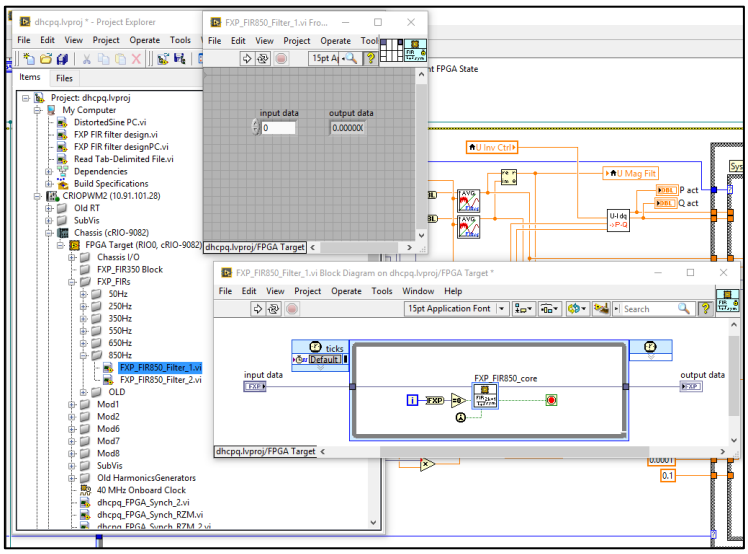


Figure 8-6: LABVIEW – Overview of the Filter VI created by the IP Generator

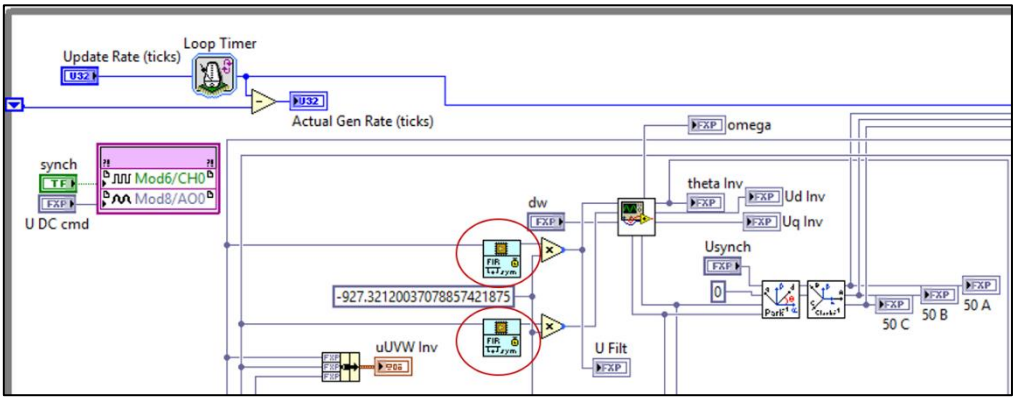


Figure 8-7: LABVIEW – Inserted FIR Filter VIs in the Main Program Code

8.4.2 Simplified RT PI Controller

LABVIEW proposes multiples controllers structures including the PID controllers in its Control & Simulation palette. However, a simple PI controller (widely used) does not exist, if it is not a normal PID controller with a zero derivative time constant.

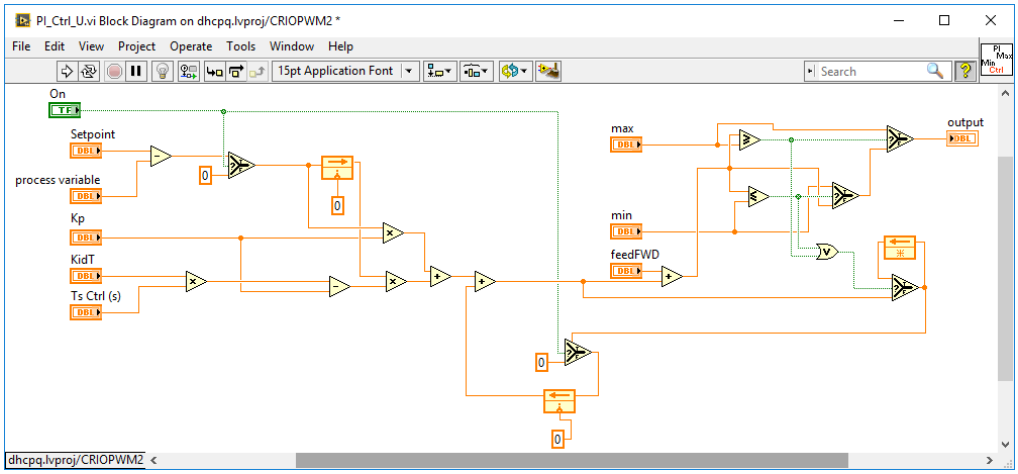


Figure 8-8: LABVIEW – Constructed RT PI Controller VI

The output value c of the developed and used discrete PI controller in this project has the following structure defined in (8-1) with k_p and k_i as the controllers tuning parameters, T_s the sampling time and e the error to be corrected:

$$c(t_k) = c(t_{k-1}) + k_p \cdot e(t_k) + (k_i \cdot T_s - k_p) \cdot e(t_{k-1}) \qquad (8\text{-}1)$$

The Figure 8-8 gives an overview of the PI controller VI implemented in the RT that includes additional features like the output limitation, a reset button and an accelerating feed-forward value.

8.4.3 Inverter Frame-based Voltages Synchronisation

The Figure 8-9 shows the LABVIEW program implementing the voltage sources synchronisation method based on the inverter dq-frame detailed in the paragraph 5.5.2.2. It is a sequential process, where first the voltage magnitude is controlled then the phase-shift. The phase-shift control start after the voltage magnitude difference becomes less than 10 volts. In order to ensure that the system reaches a steady synchronism state, each controller computational error must remain below a defined range for a given time constant. In this program, running at 2 kHz, the system should remain in its steady states for 400 iterations. This means 1/5 second or 10 cycles of the fundamental 50 Hz signal.

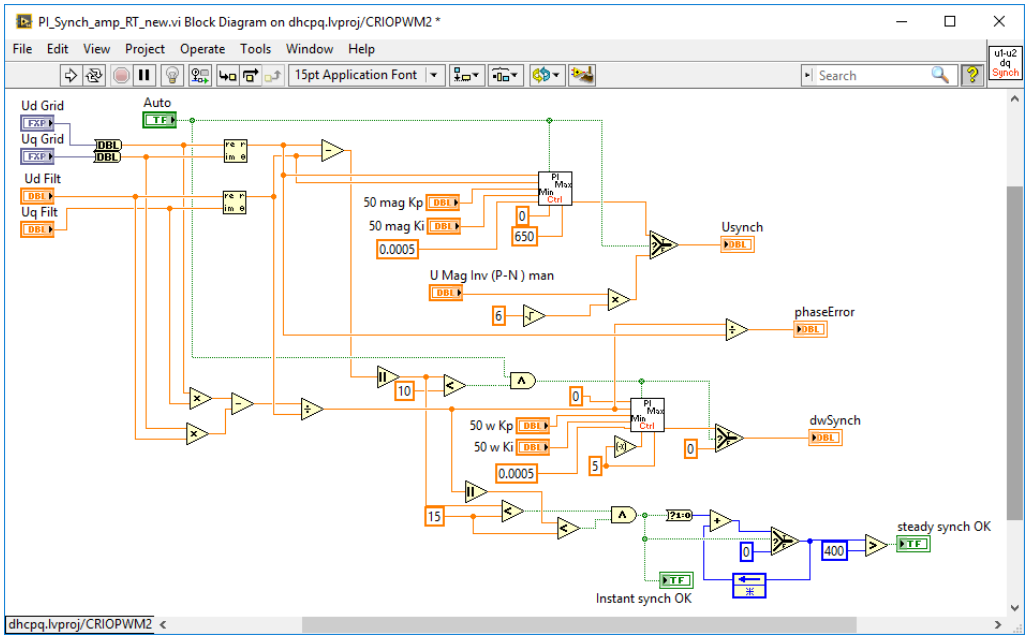


Figure 8-9: LABVIEW – Built up RT Voltages Synchronism Controller

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